Analog Electronics
ENEE236

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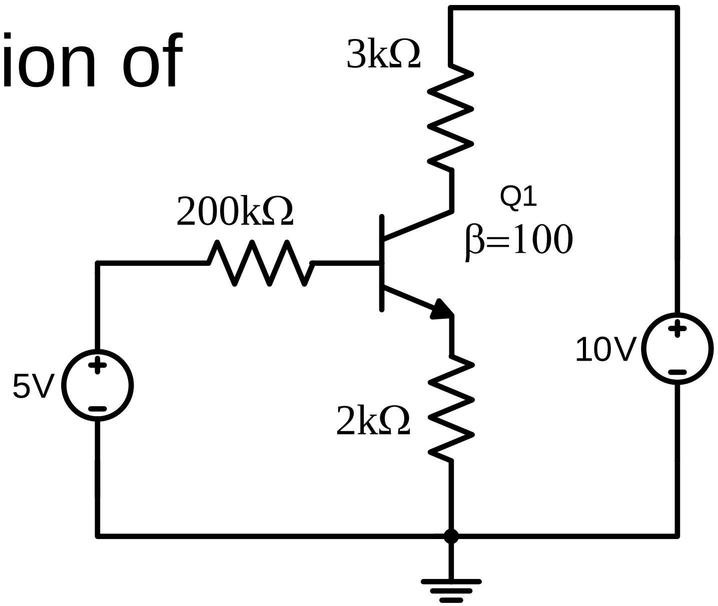
L8- DC Biasing - BJTs

Example

- Assume $V_{CE(sat)}$=0.2 V
- Find mode of operation of Q1 ?



Determine Mode of Operation of BJT?

- Solution:
- 1) Since BE junction is forward biased ==> Q1 can be either in Active (Linear) or Saturation mode
- Assume it is in Active Mode

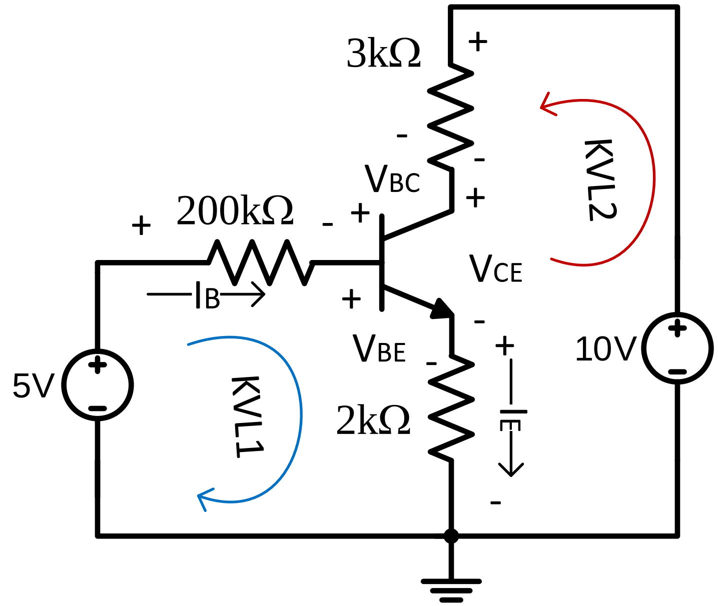
$$5 = 200\ \text{k}\Omega \,.\, I_B + V_{BE} + 2\ \text{k}\Omega .\, I_E$$

But, $$I_E = (1+\beta) I_B$$

$$\text{Solve for } I_B = \frac{5 - V_{BE}}{200\ \text{k}\Omega + (1+\beta) .\, 2\ \text{k}\Omega}$$

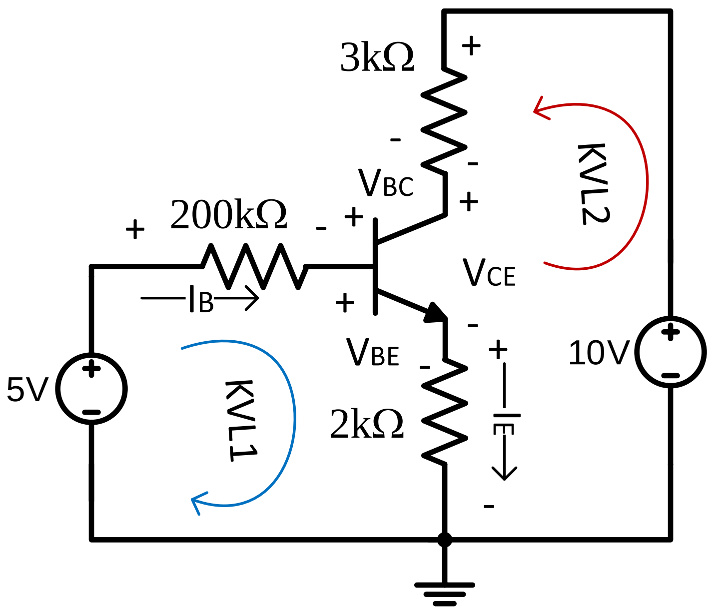
$$I_B = \frac{5 - 0.7}{200\ \text{k}\Omega + (1+100) .\, 2\ \text{k}\Omega}$$

$$= \frac{4.3\ \text{V}}{402\ \text{k}\Omega} = 10.7\ \mu\text{A}$$



$$I_C = \beta I_B$$
$$= (100).(10.7\ \mu A)$$
$$= 1.07\ \ mA$$
$$I_E = (\beta + 1) I_B$$
$$= 1.0807\ mA$$

Now we find V_{CE} from output circuit



$$10 - I_C .3\ k\Omega - I_E .2\ k\Omega = V_{CE}$$
$$\Rightarrow V_{CE} = 4.63\ V > V_{CE(sat)}$$

$\therefore$ Q1 is in active mode and the assumption is true

we can also verify that the BC junction is reverse biassed which is required so that the BJT operates in active mode

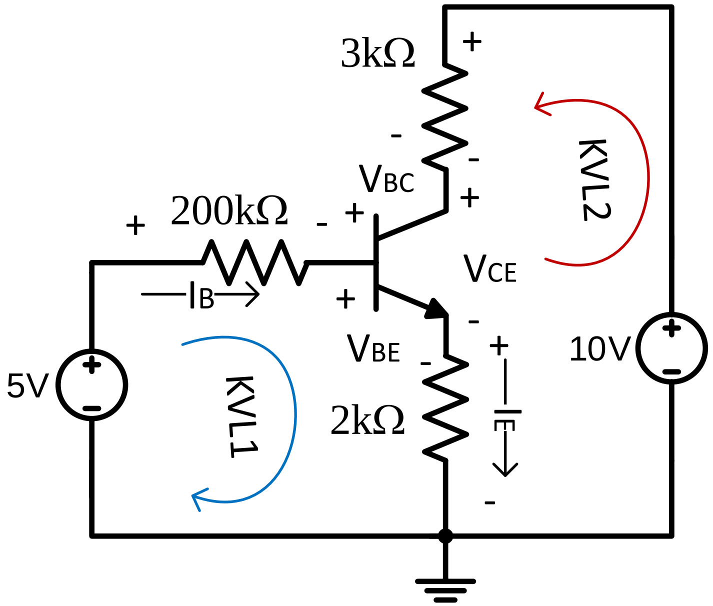
$$10 - I_C \,.3\,k\Omega - I_E \,.2\,k\Omega = V_{CE}$$

$$\Rightarrow V_{CE} = V_{CB} - V_{EB}$$

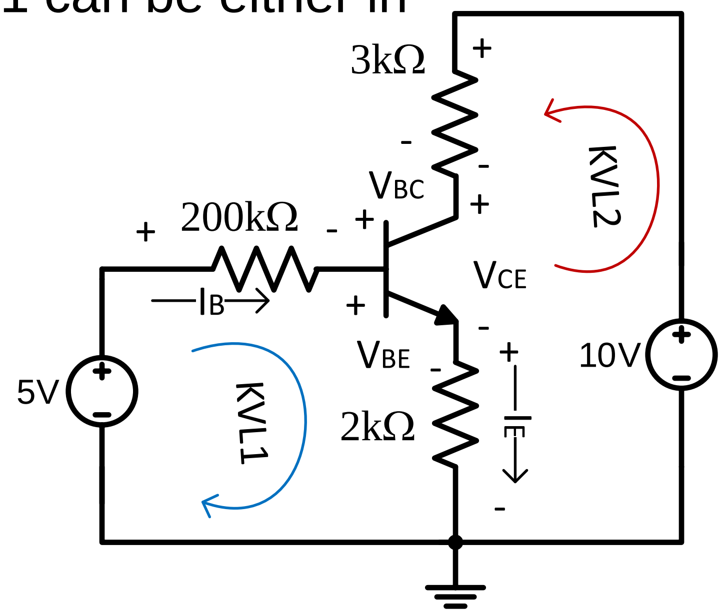
$$\Rightarrow V_{CB} = V_{CE} - V_{BE} = 4.63 - 0.7 = 3.93\,V$$

$$\therefore V_{BC} = -V_{CB} = -3.33\,V$$

BC junction is reverse biased



- Solution:
- 1) Since BE junction is forward biased ==> Q1 can be either in Active (Linear) or Saturation mode
- Assume it is in saturation mode:



$$10 - I_{C(sat)}.3k\Omega - I_{E(sat)}.2k\Omega = V_{CE(Sat)}$$

$$\text{assume} \quad I_{E(sat)} = I_{C(sat)}$$

$$\therefore I_{C(sat)} = \frac{10-0.2}{5k\Omega} = 1.96 \ \text{mA}$$

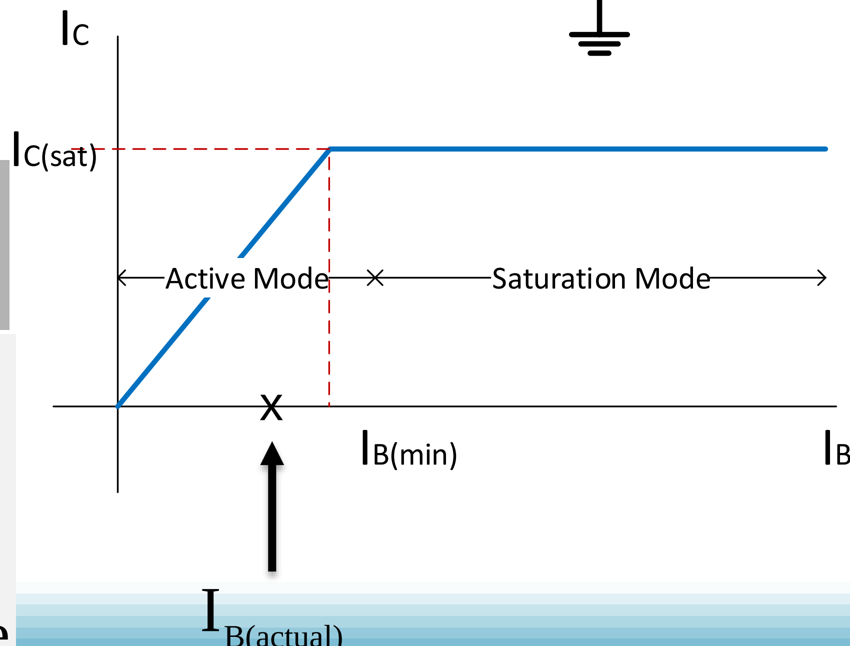
$$I_{B(min)} = \frac{I_{C(sat)}}{\beta} = 19.6 \ \mu A$$

Now we find the actual value of IB

$I_{B(actual)} = 10.7 \, \mu A$ (it was found previously)

since

$I_{B(actual)} < I_{B(sat)} = I_{B(min)} \Rightarrow$ the assumption made earlier that BJT in saturation mode is wrong , and actually it is in active mode

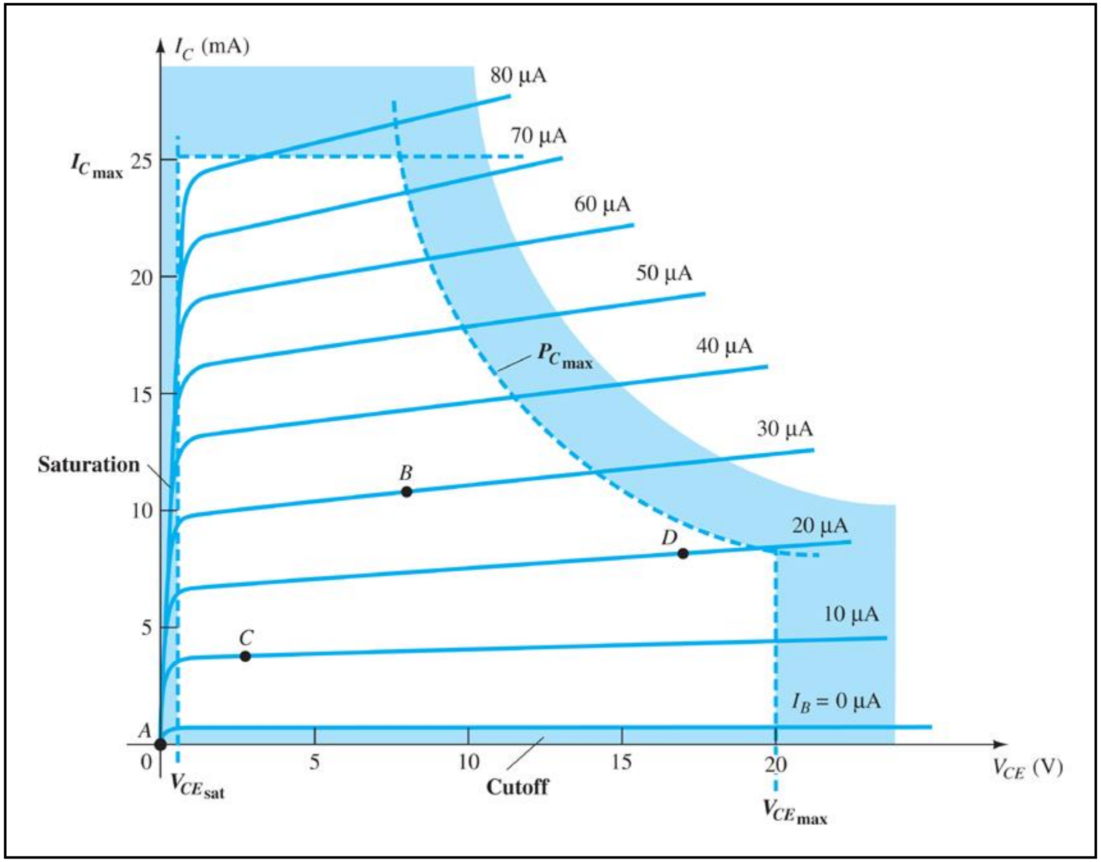


Biasing

Biasing: Applying DC voltages to a transistor in order to establish fixed level of voltage and current.
For Amplifier (active/Linear) mode, the resulting dc voltage and current establish the operation point to turn it on so that it can amplify AC signals.

Operating Point

The DC input establishes an operating or *quiescent point* called the ***Q-point***.



The Three Operating Regions

Active or Linear Region Operation

- Base–Emitter junction is forward biased
- Base–Collector junction is reverse biased

Cutoff Region Operation

- Base–Emitter junction is reverse biased

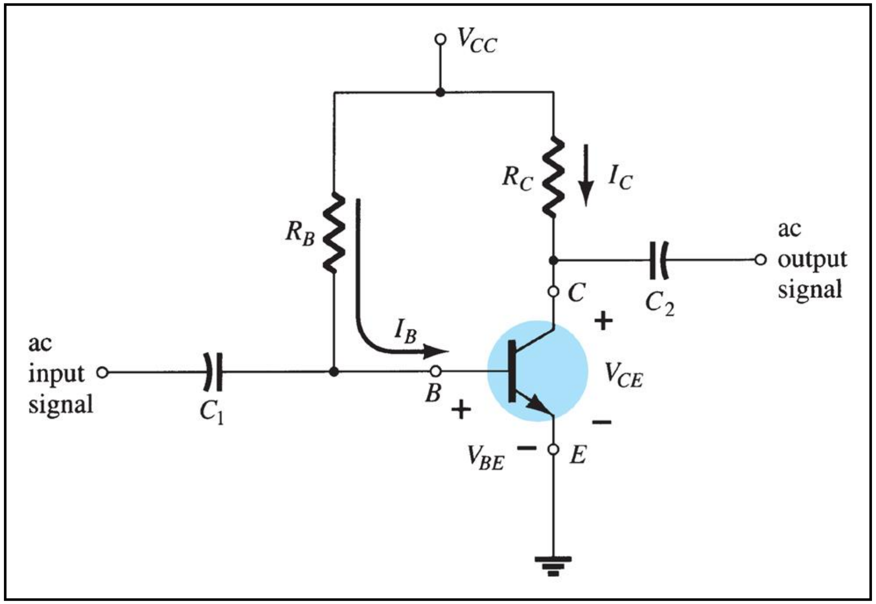
Saturation Region Operation

- Base–Emitter junction is forward biased
- Base–Collector junction is forward biased

DC Biasing Circuits

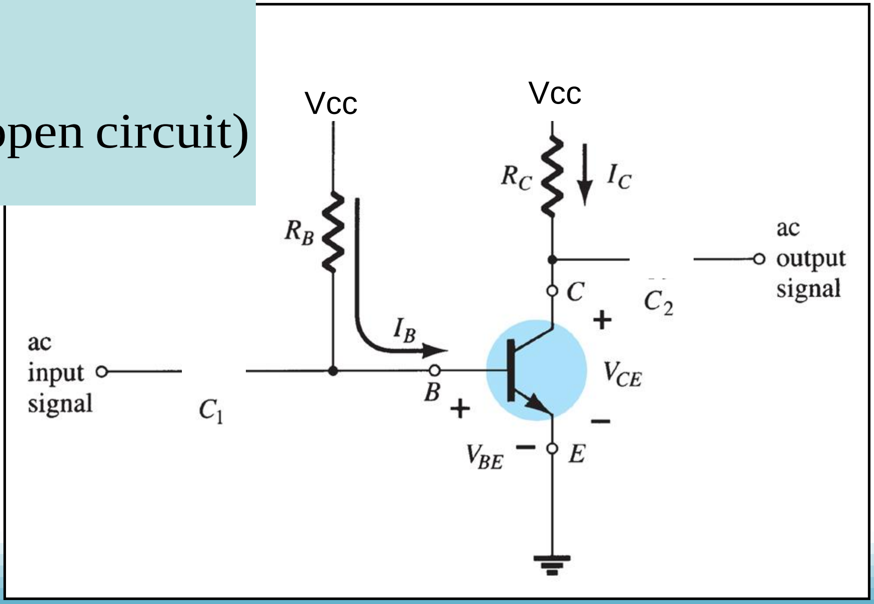
1. Fixed-bias circuit
2. Emitter-stabilized bias circuit
3. DC bias with voltage feedback
4. Voltage divider bias circuit

1)Fixed Bias Configuration



DC equivalent circuit

$$f = 0 \Rightarrow Xc = \frac{1}{2\pi fC} \cong \infty \text{ (open circuit)}$$



The Base-Emitter Loop

From Kirchhoff's voltage law for Input:

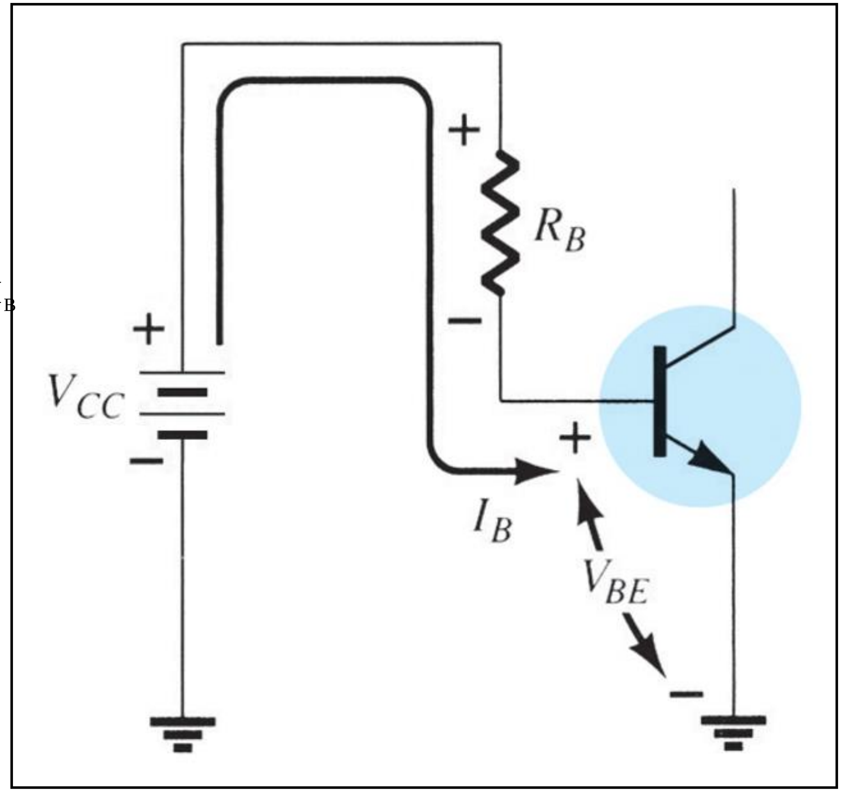
$$+V_{CC} - I_B R_B - V_{BE} = 0$$

Solving for base current:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

Choosing R_B will establish the required level of I_B

I_B



Collector-Emitter Loop

Collector current:

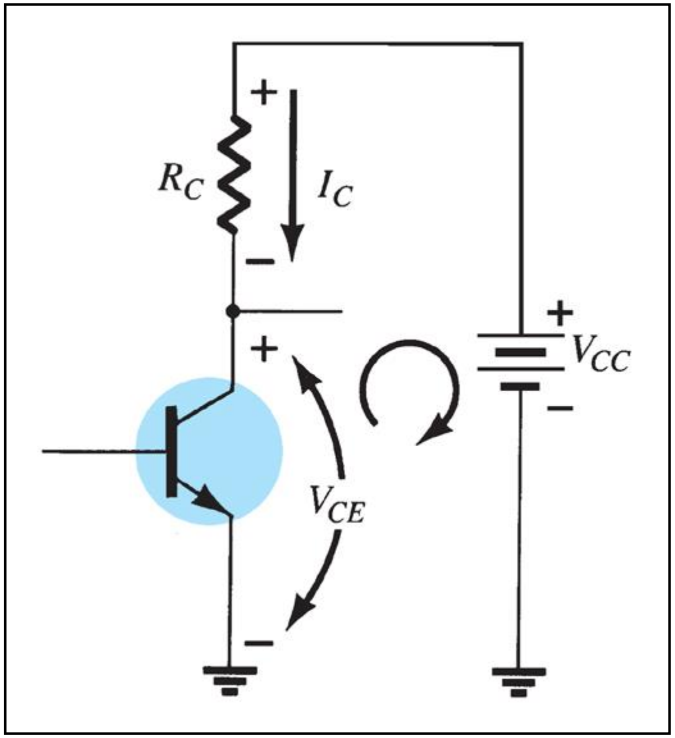
$$I_C = \beta I_B$$

From Kirchhoff's voltage law:

$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{CE} = V_C - V_E$$

$$\text{Since } V_E = 0 \Rightarrow \therefore V_{CE} = V_C$$

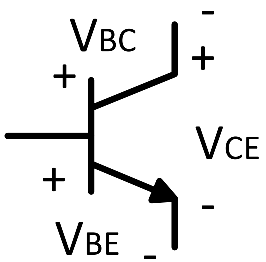


$$V_{CE} = V_{CC} - I_C R_C$$

Also

$$V_{BE} = V_B - V_E$$

$$\therefore V_{BE} = V_B$$



$$V_{BE} - V_{CE} - V_{BC} = 0$$

$$\therefore V_{BC} = V_{BE} - V_{CE}$$

Saturation

When the transistor is operating in **saturation**, current through the transistor is at its *maximum* possible value.

$$I_{Csat} = \frac{V_{CC}}{R_C}$$

$$V_{CE} = V_{CE(sat)} \cong 0\ V$$

Load Line Analysis

The load line end points are:

I_{Csat}

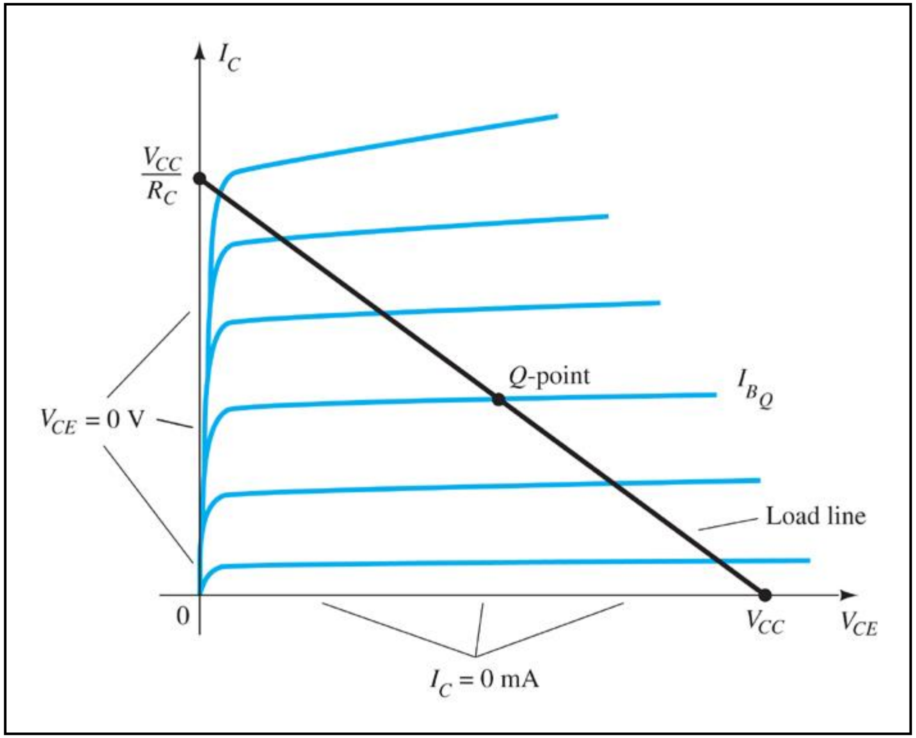
$I_C = V_{CC} / R_C$

$V_{CE} = 0$ V

$V_{CEcutoff}$

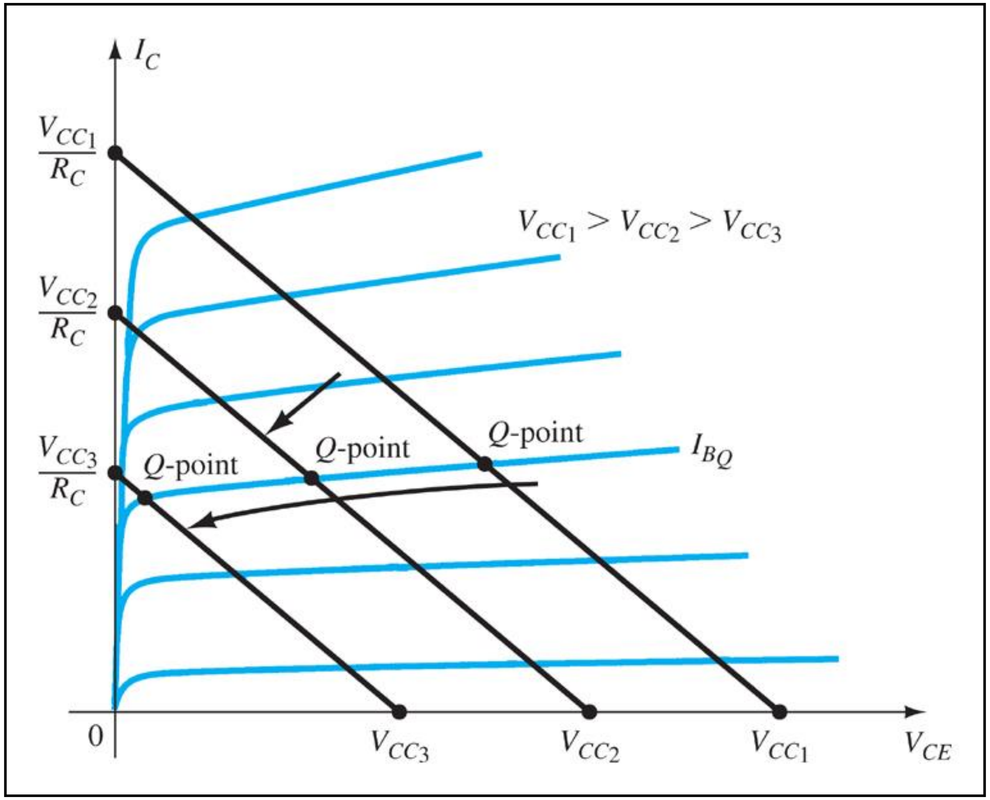
$V_{CE} = V_{CC}$

$I_C = 0$ mA

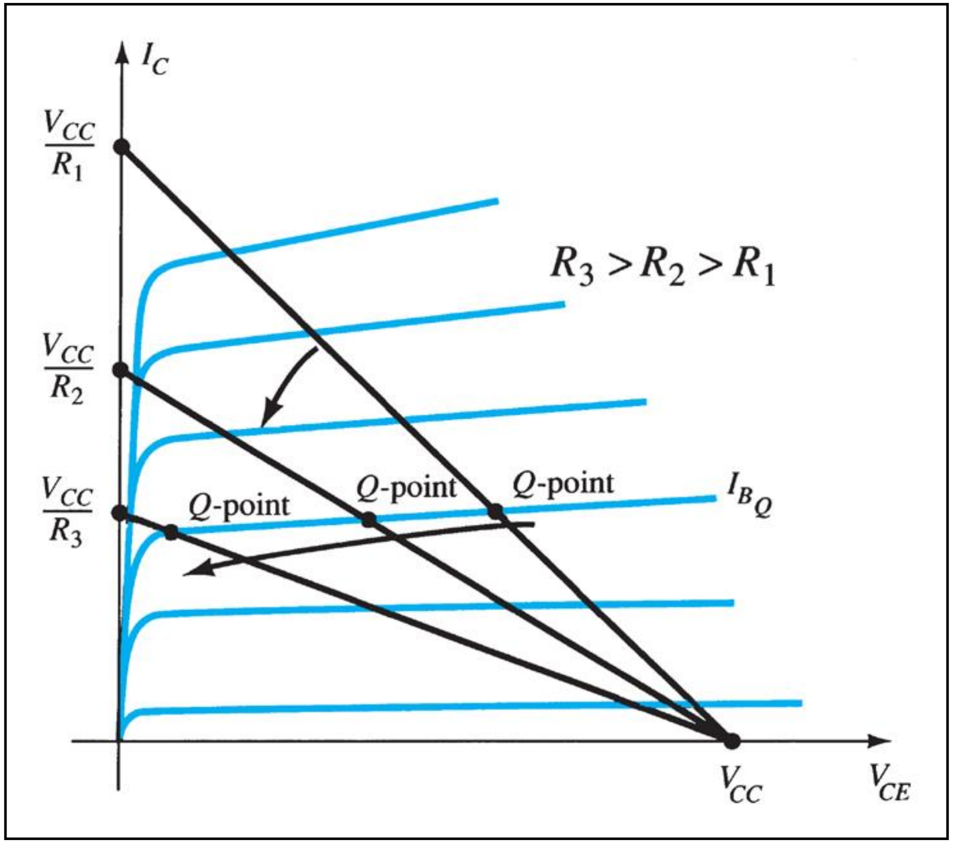


The *Q*-point is the operating point where the value of R_B sets the value of I_B that controls the values of V_{CE} and I_C.

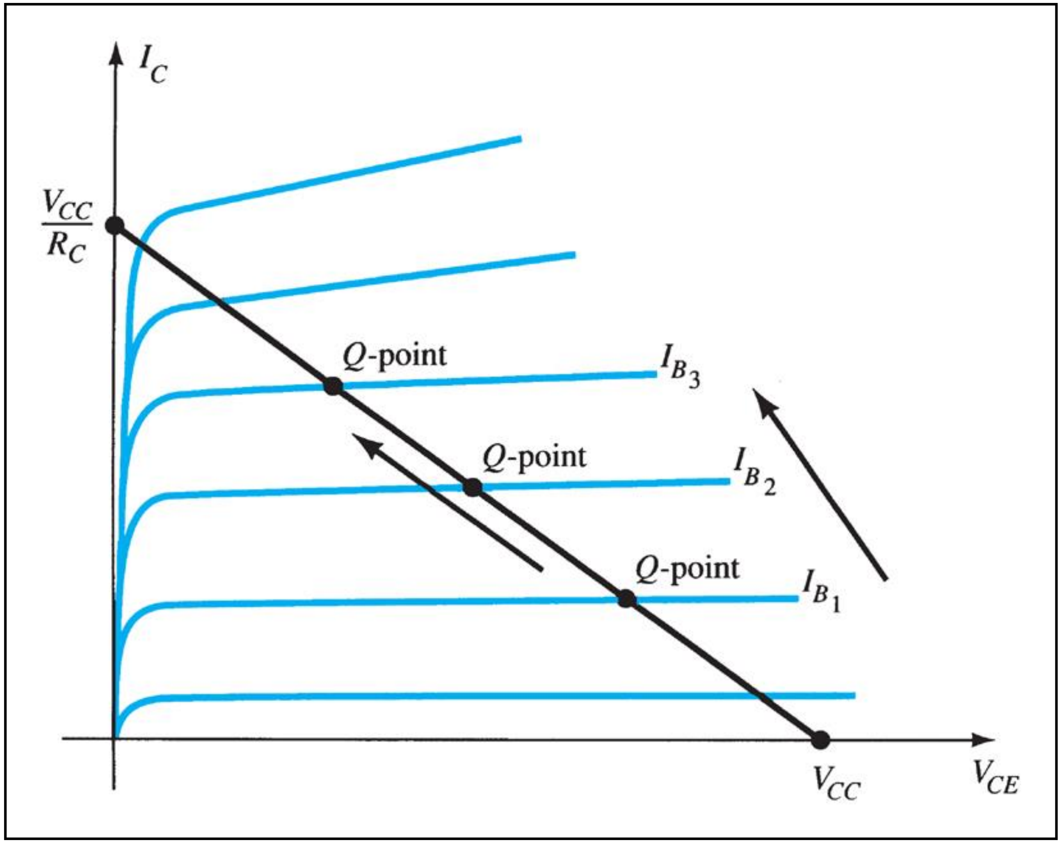
The Effect of V_{CC} on the Q-Point



The Effect of R_C on the Q-Point



The Effect of I_B on the Q-Point



Design: Fixed bias

$$\text{Assume VCC} = 10\text{V},\ \beta_{\text{nominal}} = 100,\ \beta_{\text{min}} = 50,\ \beta_{\text{max}} = 150$$

$$\text{Design for Q-point}: V_{CEQ} = 5\text{V},\ I_{CQ} = 1\text{mA}$$

Solution

$$I_{BQ} = \frac{I_{CQ}}{\beta_{\text{nominal}}} = \frac{1\,\text{mA}}{100} = 10\,\mu\text{A}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \Rightarrow$$

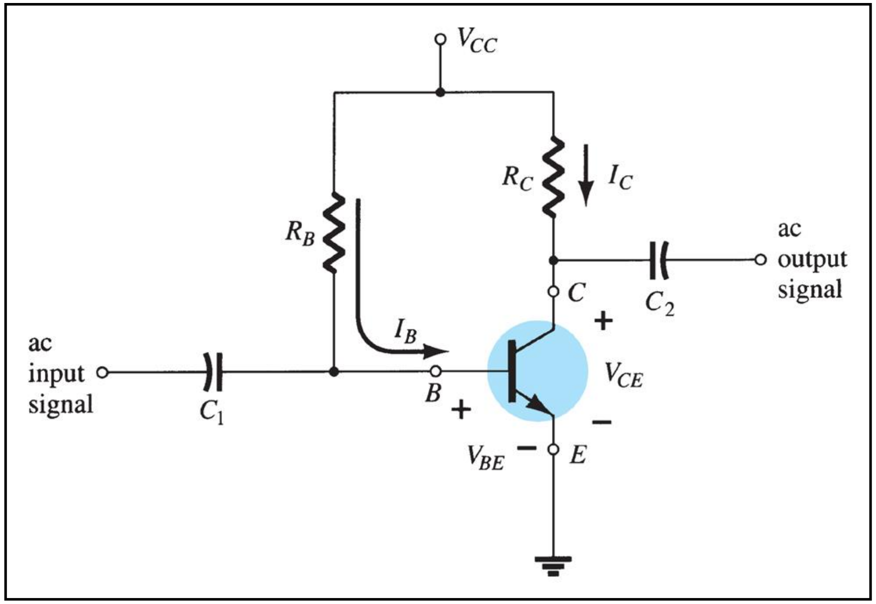
$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{10 - 0.7}{10\,\mu\text{A}}$$

$$= 930\,\text{k}\Omega$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{CEQ} = 5 = 10 - I_C R_C$$

$$\therefore\ R_C = \frac{5}{1\,\text{mA}} = 5\,\text{k}\Omega$$



Fixed bias Stability

$\text{Assume VCC} = 10\text{V},\ \beta_{nominal} = 100,\ \beta_{min} = 50,\ \beta_{max} =$

$\text{Design for Q-point: } V_{CEQ} = 5\text{V},\ I_{CQ} = 1\text{mA}$

Solution – continued

$$\text{If } \beta = \beta_{min} = 50$$

$$I_B = 10\ \mu\text{A}$$

$$I_C = \beta I_B = (50)(10\ \mu\text{A}) = 0.5\ \text{mA}$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{CEQ} = 10 - (0.5\ \text{mA})(5\ \text{k}\Omega) = 7.5\ \text{V}$$

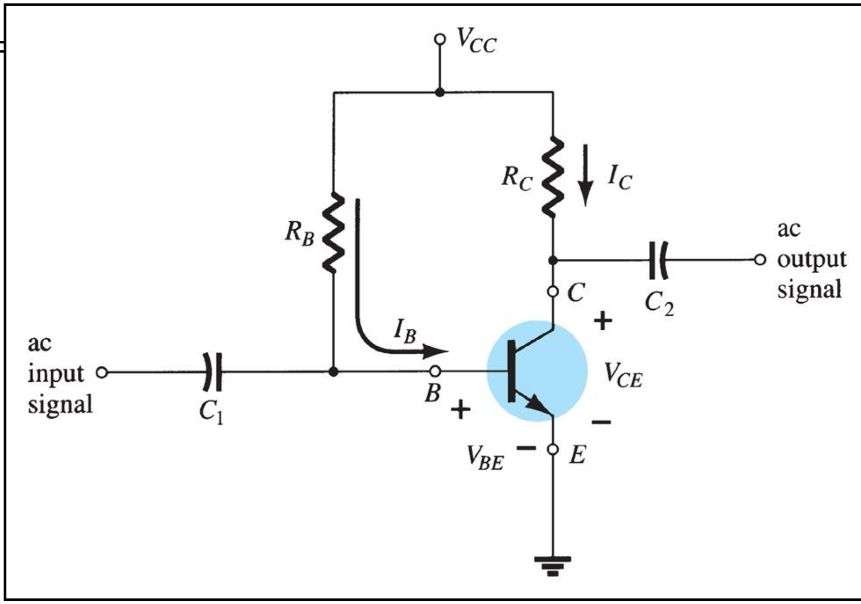
$$\text{If } \beta = \beta_{max} = 150$$

$$I_B = 10\ \mu\text{A}$$

$$I_C = \beta I_B = (150)(10\ \mu\text{A}) = 1.5\ \text{mA}$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{CEQ} = 10 - (1.5\ \text{mA})(5\ \text{k}\Omega) = 2.5\ \text{V}$$



for

$$50 \le \beta \le 150$$

$$I_B = 10\ \mu\text{A fixed}$$

$$0.5\ \text{mA} \le I_C \le 1.5\ \text{mA}$$

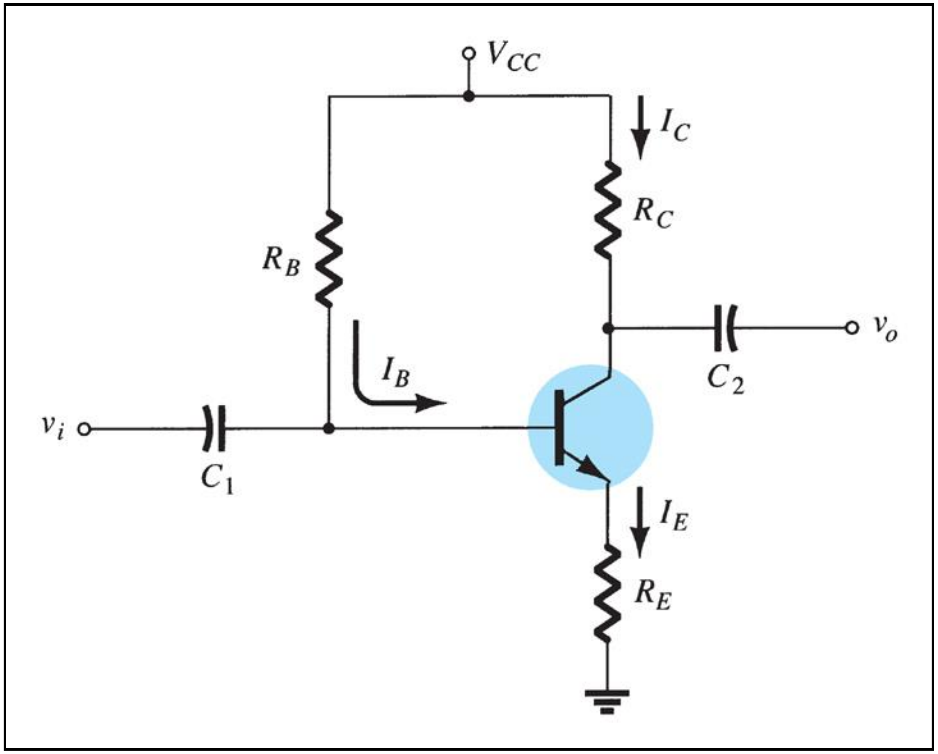
$$7.5\ \text{V} \ge V_{CE} \ge 2.5\ \text{V}$$

$$\therefore \frac{I_{C(max)}}{I_{C(min)}} = \frac{1.5\ \text{mA}}{0.5\ \text{mA}} = 3$$

Not very stable

2) Emitter-Stabilized Bias Circuit

Adding a resistor (R_E) to the emitter circuit stabilizes the bias circuit.



Base-Emitter Loop

From Kirchhoff's voltage law:

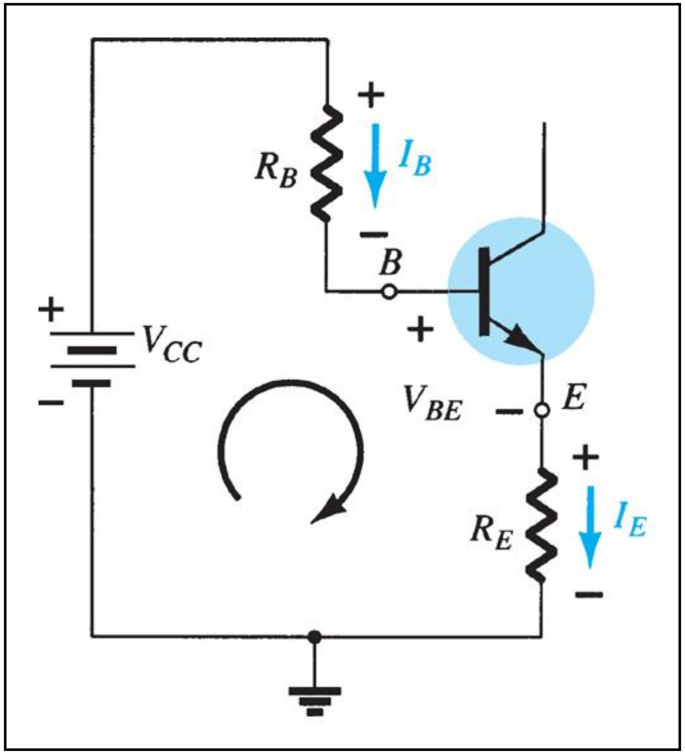
$$+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

Since $I_E = (\beta + 1) I_B$:

$$V_{CC} - I_B R_B - V_{BE} - (\beta + 1) I_B R_E = 0$$

Solving for I_B:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}$$

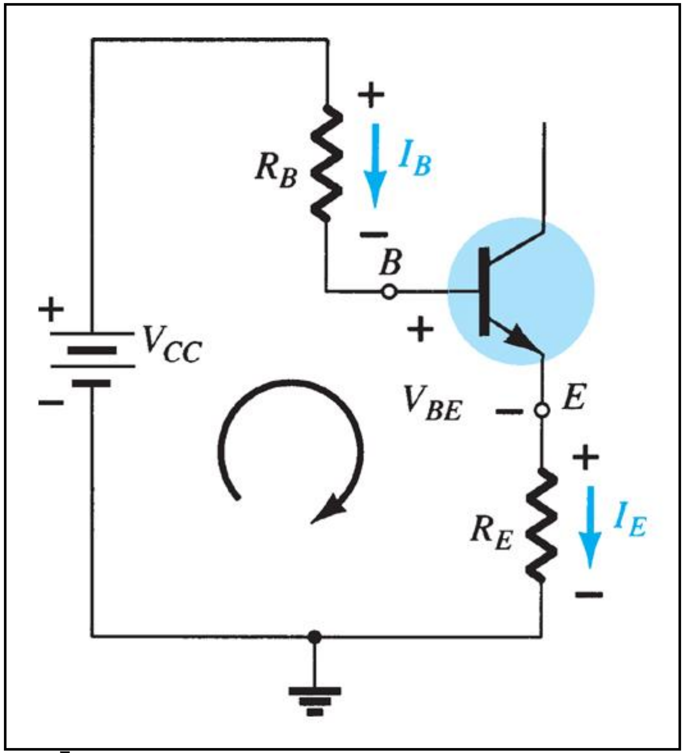


$(\beta + 1) R_E$ ← is the emitter resistor as it appears in the base emitter loop

Base-Emitter Loop

Solving for I_E:

$$I_E = \frac{V_{CC} - V_{BE}}{\frac{R_B}{(\beta + 1)} + R_E}$$



In order to get IE almost independant of B

we choose:

$$R_E >> \frac{R_B}{(\beta + 1)}$$

$$\Rightarrow I_E \cong \frac{V_{CC} - V_{BE}}{R_E}$$

Also, in order to guarantee operation in linear mode

we choose $0.1\,V_{CC} \leq V_E < 0.2V_{CC}$

Collector-Emitter Loop

From Kirchhoff's voltage law:

$$I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

Since $I_E \cong I_C$:

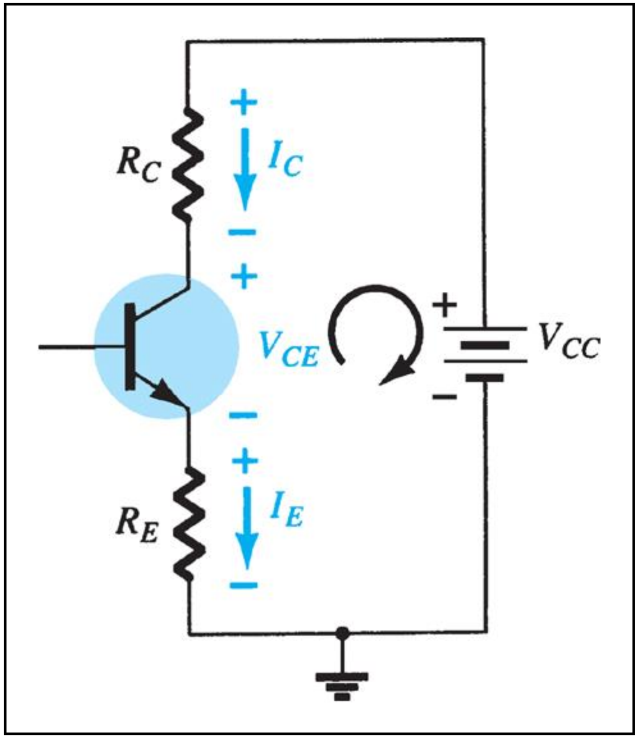
$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Also:

$$V_E = I_E R_E$$

$$V_C = V_{CE} + V_E = V_{CC} - I_C R_C$$

$$V_B = V_{CC} - I_R R_B = V_{BE} + V_E$$



Design: Emitter Stabilization bias

$$\text{Assume VCC} = 10\text{V},\ \beta_{\text{nominal}} = 100,\ \beta_{\text{min}} = 50,\ \beta_{\text{max}} = 150$$

$$\text{Design for Q-point: } V_{CEQ} = 5\text{V},\ I_{CQ} = 1\text{mA}$$

Solution

$$-\text{let } V_E = 0.1\,V_{CC}$$

$$V_E = 1\text{V}$$

$$I_E = \frac{V_E}{R_E} \Rightarrow R_E = \frac{1\,\text{V}}{1.01\,\text{mA}} \cong 1\,\text{k}\Omega$$

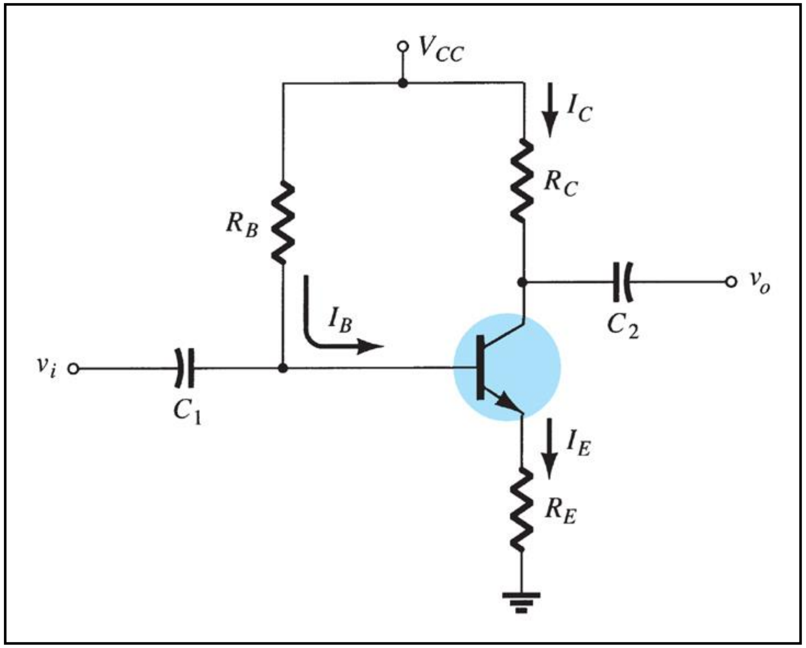
$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta+1)R_E} \Rightarrow$$

$$R_B I_B + I_B(\beta+1)R_E = V_{CC} - V_{BE}$$

$$R_B = \frac{V_{CC} - V_{BE} - I_B(\beta+1)R_E}{I_B}$$

$$= \frac{10 - 0.7 - 10\,\mu\text{A}(100+1)1\,\text{k}\Omega}{10\,\mu\text{A}}$$

$$= 829\,\text{k}\Omega$$

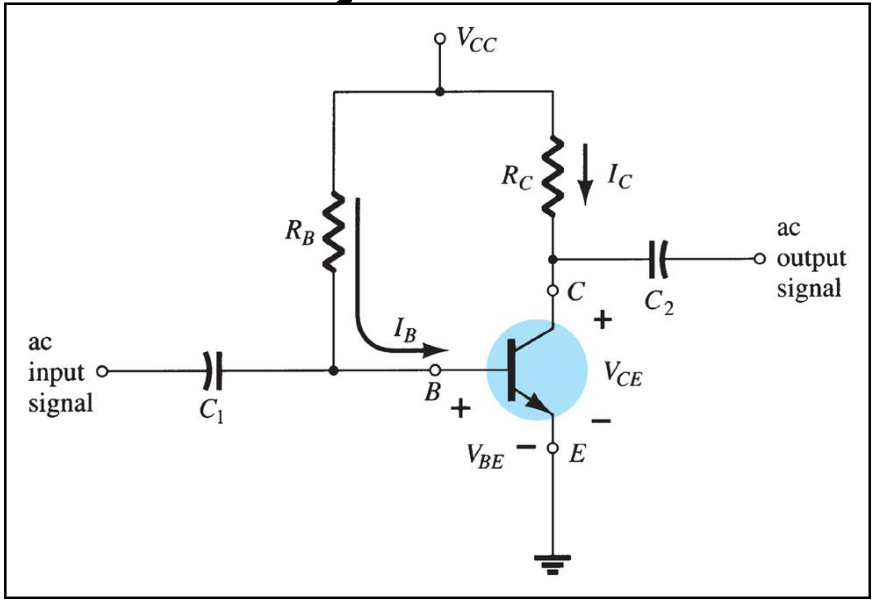


$$V_{CE} = V_{CC} - I_C R_C - V_E$$

$$V_{CEQ} = 5 = 10 - 1 - I_C R_C$$

$$\therefore\ R_C = \frac{4}{1\,\text{mA}} = 4\,\text{k}\Omega$$

Emitter bias Stability



$$\text{If } \beta = \beta_{min} = 50$$

$$I_B = \frac{9.3}{829k\Omega + 51k\Omega} = 10.56\,\mu A$$

$$I_C = \beta I_B = (50)(10.56\,\mu A) = 0.528\,mA$$

$$V_{CE} = V_{CC} - I_C R_C - V_E$$

$$V_{CEQ} = 10 - (0.528\,mA)(4\,k\Omega) - 1 = 6.89\,V$$

$$\text{If } \beta = \beta_{max} = 150$$

$$I_B = \frac{9.3}{829k\Omega + 151k\Omega} = 9.489\,\mu A$$

$$I_C = \beta I_B = (150)(9.489\,\mu A) = 1.423\,mA$$

$$V_{CE} = V_{CC} - I_C R_C - V_E$$

$$V_{CEQ} = 10 - (1.423\,mA)(4\,k\Omega) - 1 = 3.31\,V$$

for

$$50 \le \beta \le 150$$

$$10.56\,\mu A \ge I_B \ge 9.489\,\mu A$$

$$0.528\,mA \le I_C \le 1.423\,mA$$

$$6.89\,V \ge V_{CE} \ge 3.31\,V$$

$$\therefore \frac{I_{C(max)}}{I_{C(min)}} = \frac{1.423\,mA}{0.528\,mA} \cong 2.7$$

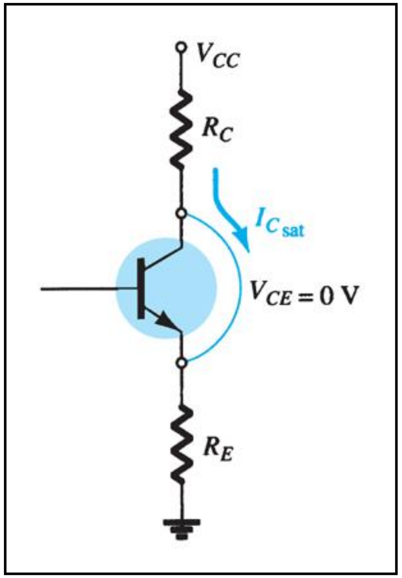
Improved, but not very stable

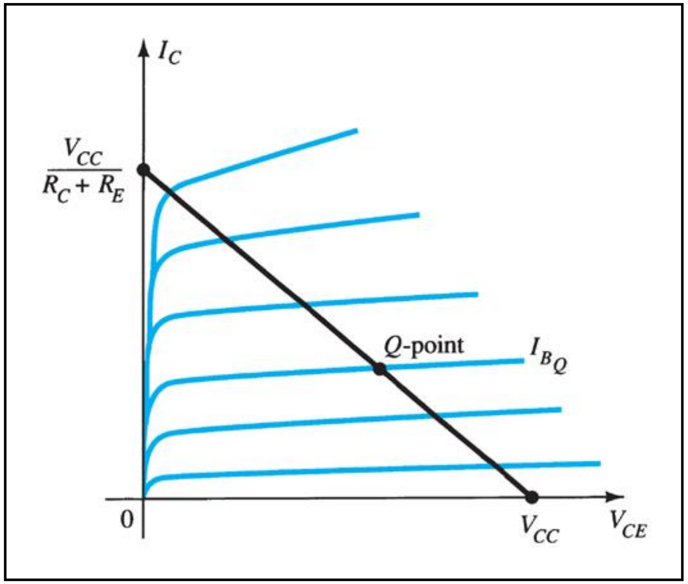
Improved Biased Stability

Stability refers to a condition in which the currents and voltages remain fairly constant over a wide range of temperatures and transistor Beta (β) values.

Adding R_E to the emitter improves the stability of a transistor.

Saturation Level





The endpoints can be determined from the load line.

$V_{CEcutoff}$:

$$V_{CE} = V_{CC}$$
$$I_C = 0 \text{ mA}$$

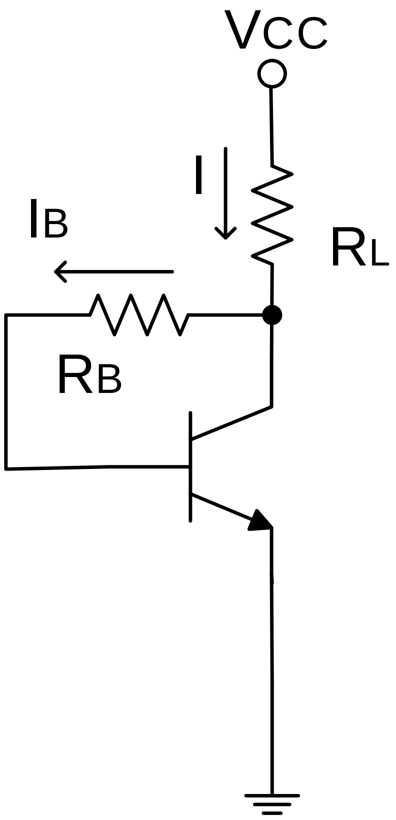
I_{Csat}:

$$V_{CE} = 0 \text{ V}$$
$$I_C = \frac{V_{CC}}{R_C + R_E}$$

3) DC Bias With Voltage Feedback

Another way to improve the stability of a bias circuit is to add a feedback path from collector to base.

In this bias circuit the Q-point is only slightly dependent on the transistor beta, β.



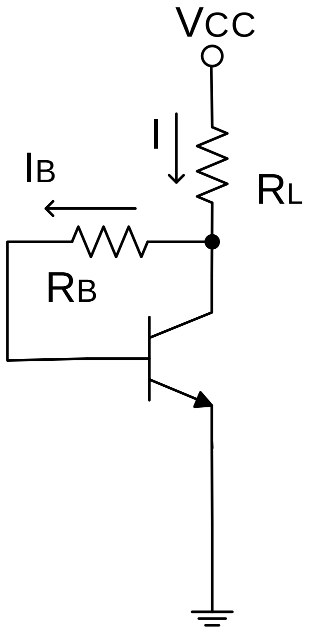
Base-Emitter Loop

From Kirchhoff's voltage law:

$$V_{CC} - I.R_L - I_B R_B - V_{BE} = 0$$
$$I = I_C + I_B$$
$$I_C = \beta I_B$$

Solving for I_B:

$$I_B = \frac{V_{CC} - V_{BE}}{R_L(\beta + 1) + R_B}$$



$$V_{CC} = I.R_L + V_{CE}$$
$$I = I_C + I_B$$
$$V_{CE} = V_{CC} - (I_C + I_B)R_L$$

suppose $\beta\uparrow, I_B\downarrow, I_C = \uparrow\beta.I_B\downarrow \cong \text{const}$

there is some kind of compensation effect

Design: Voltage feedback bias

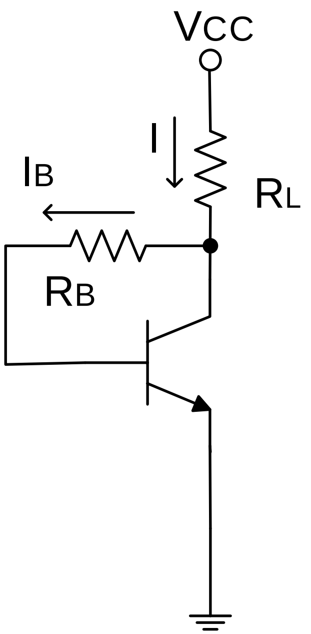
$$\text{Assume VCC} = 10\text{V},\ \beta_{nominal} = 100,\ \beta_{min} = 50,\ \beta_{max} = 150$$

$$\text{Design for Q-point}: V_{CEQ} = 5\text{V},\ I_{CQ} = 1\text{mA}$$

Solution

$$R_L = \frac{V_{CC} - V_{CE}}{I_C + I_B} = \frac{10-5}{1\text{mA} + \frac{1\text{mA}}{100}}$$

$$= 4.95\ \text{k}\Omega$$



$$I_B = \frac{V_{CC} - V_{BE}}{R_L(\beta+1) + R_B}$$

$$\therefore R_B = 430\ \text{k}\Omega$$

$$\text{If } \beta = \beta_{min} = 50$$

$$I_B = 0.013627\ \text{mA}$$

$$I_C = 0.68\ \text{mA}$$

$$\text{If } \beta = \beta_{max} = 150$$

$$I_B = 0.00793\ \text{mA}$$

$$I_C = 1.19\ \text{mA}$$

for

$$50 \le \beta \le 150$$

$$0.68\ \text{mA} \le I_C \le 1.19\ \text{mA}$$

$$\therefore \frac{I_{C(max)}}{I_{C(min)}} = \frac{1.19\ \text{mA}}{0.68\ \text{mA}} \cong 1.75$$

Better Q-point stability

Base-Emitter Bias Analysis

Transistor Saturation Level

$$I_{Csat} = I_{Cmax} = \frac{V_{CC}}{R_L}$$

Load Line Analysis

Cutoff

$$V_{CE} = V_{CC}$$

$$I_C = 0\,mA$$

Saturation

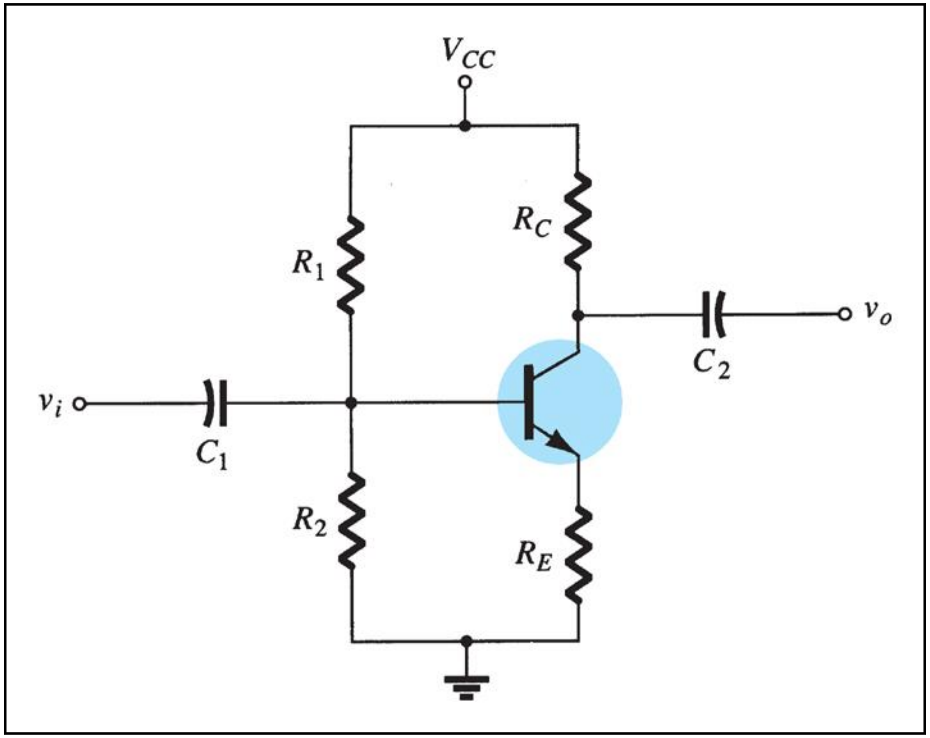
$$I_C = \frac{V_{CC}}{R_L}$$

$$V_{CE} = 0\text{ V}$$

4) Voltage Divider Bias

This is a very stable bias circuit.

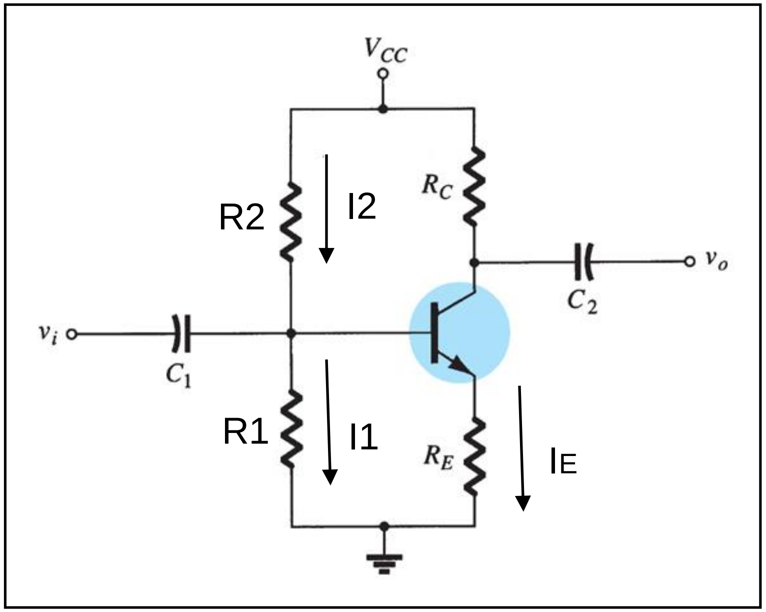
The currents and voltages are nearly independent of any variations in β if the circuit is designed properly



Approximate Analysis

Where $I_B \ll I_1$ and $I_1 \cong I_2$:

$$V_B = \frac{R_1 V_{CC}}{R_1 + R_2}$$



$$V_E = V_B - V_{BE}$$

$$I_{E(approximate)} = \frac{V_E}{R_E} = \frac{V_B - V_{BE}}{R_E}$$

From Kirchhoff's voltage law:

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$I_E \cong I_C$$

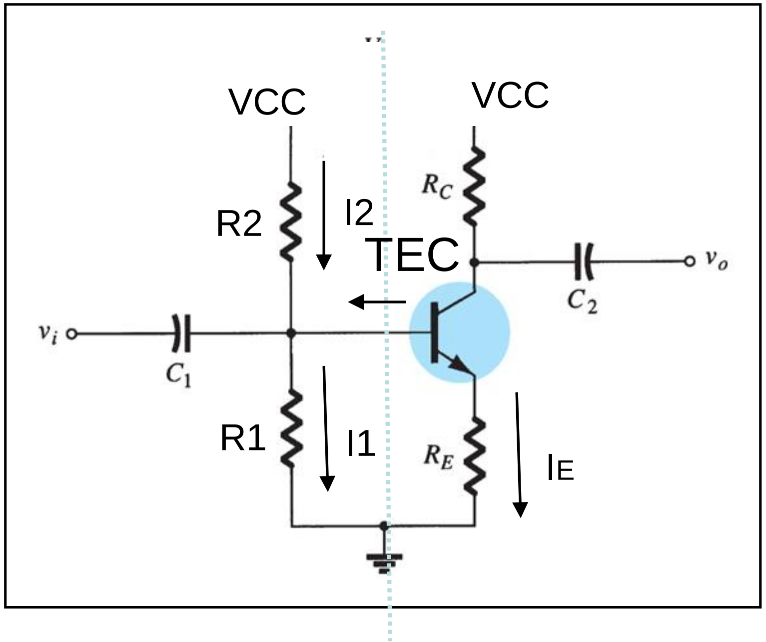
$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Here we got Ic independent of β which provides good Q-point stability

Exact Analysis

We must try to make I_B as close as possible to zero

Thevenin Equivalent circuit for the circuit left of the base is done



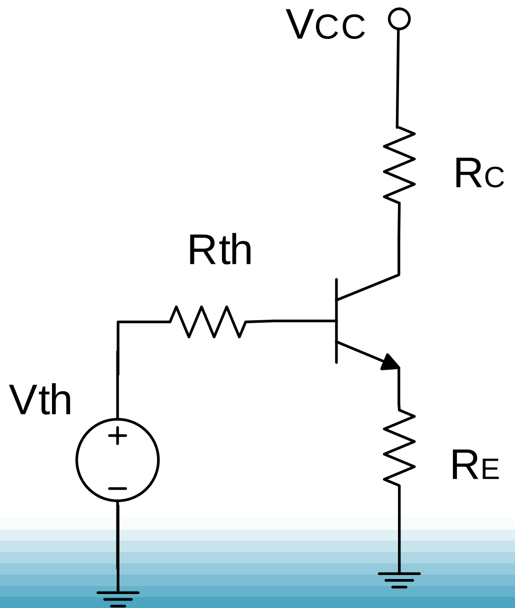
$$V_{th} = \frac{R_1 V_{CC}}{R_1 + R_2}$$

$$R_{th} = R_1 // R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

$$V_{th} = I_B R_{th} + V_{BE} + I_E R_E$$

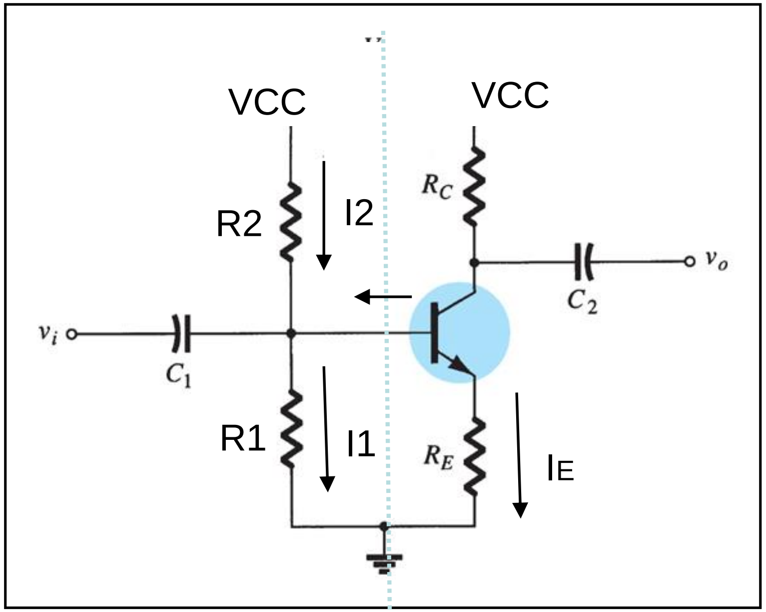
$$\text{but } I_B = \frac{I_E}{\beta + 1}$$

$$\therefore I_{E(exact)} = \frac{V_{th} - V_{BE}}{\frac{Rth}{\beta + 1} + R_E}$$



Exact Analysis

$$\therefore I_{E(exact)} = \frac{V_{th} - V_{BE}}{\frac{Rth}{\beta+1} + R_E}$$



if we compare to approximate solution

$$I_{E(approximate)} = \frac{V_B - V_{BE}}{R_E}$$

$$\Rightarrow \text{we must make the quantity } \frac{Rth}{\beta+1} << R_E$$

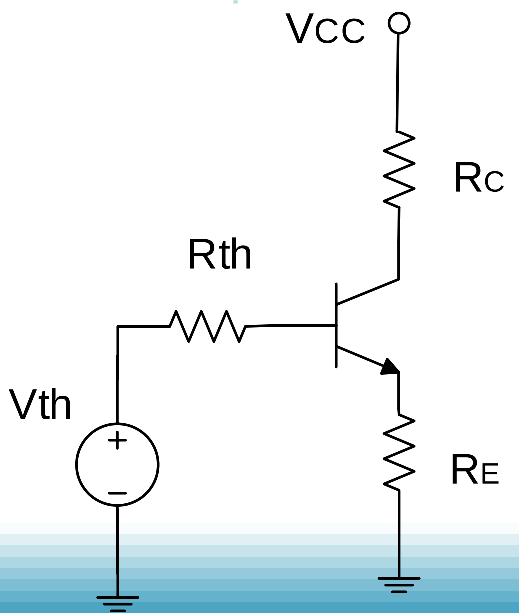
Here we got Ic independent of β

$$\therefore \quad Rth << (\beta+1)R_E$$

$$\text{as a rule let } Rth << \frac{(\beta+1)R_E}{10}$$

or

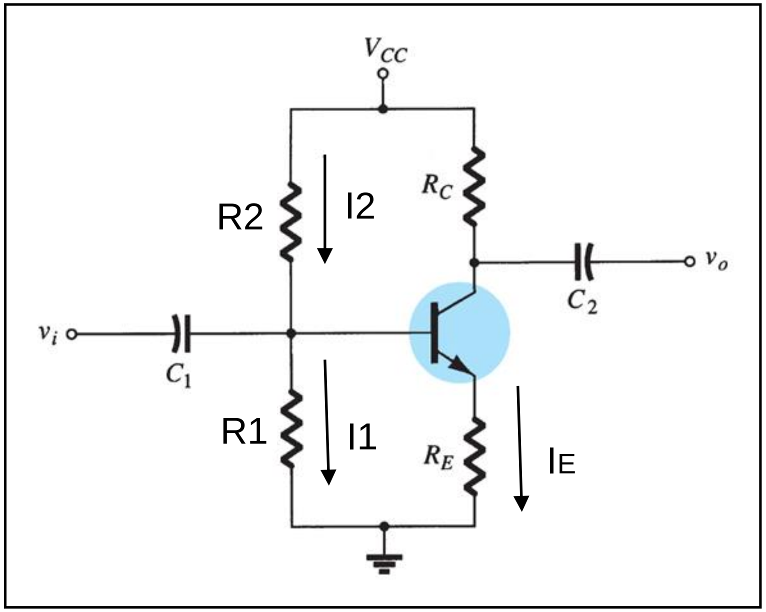
$$Rth << \frac{\beta R_E}{10}$$



Design: Voltage Divider bias

Assume $VCC = 10V,\ \beta_{nominal} = 100,\ \beta_{min} = 50,\ \beta_{max} = 150$

Design for Q-point : $V_{CEQ} = 5V,\ I_{CQ} = 1mA$



Solution

1)let $V_E = 0.1\,V_{CC}$

$V_E = 1V$

$$I_E = \frac{V_E}{R_E} \Rightarrow R_E = \frac{1\,V}{1.01\,mA} \cong 1\,k\Omega$$

2) let $Rth = \frac{R_E.\beta_{nominal}}{50} = \frac{1\,k\Omega.100}{50} = 2\,k\Omega$

3) $V_{CC} = R_C I_C + I_E R_E + V_{CE}$

$V_{CEQ} = 5$

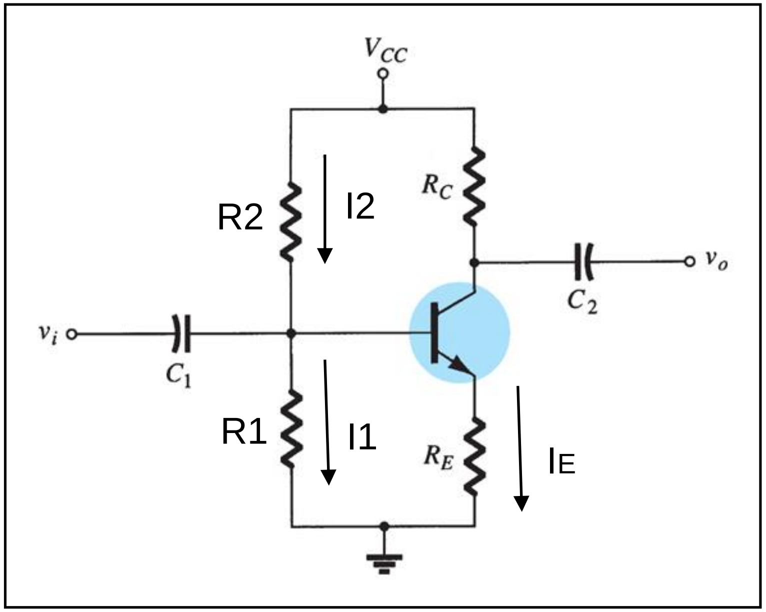
$$\therefore R_C = \frac{V_{CC} - V_{CE} - V_E}{1mA} = \frac{10 - 5 - 1}{1\,mA} = 4\,k\Omega$$

Design: Voltage Divider bias

Assume $VCC = 10V,\ \beta_{nominal} = 100,\ \beta_{min} = 50,\ \beta_{max} = 150$

Design for Q-point: $V_{CEQ} = 5V,\ I_{CQ} = 1mA$

Solution – continued



$$4)\ I_E = \frac{V_{th} - V_{BE}}{\frac{Rth}{\beta+1} + R_E}$$

$$\therefore V_{th} = \frac{R_1 V_{CC}}{R_1 + R_2} = I_E\left(\frac{Rth}{\beta+1} + R_E\right) + V_{BE} = 1.72V \quad ...(1)$$

$$R_{th} = R_1 // R_2 = \frac{R_1 R_2}{R_1 + R_2} = 2\ k\Omega \qquad ....(2)$$

solving (1) & (2) yields:

$R_1 = 2.42\ k\Omega$

$R_2 = 11.64\ k\Omega$

Voltage Divider bias Stability

$$\text{If } \beta = \beta_{\min} = 50$$

$$I_C = 0.982\,\text{mA}$$

$$\text{If } \beta = \beta_{\max} = 150$$

$$I_C = 1.0069\,\text{mA}$$

$$\text{for}$$

$$50 \le \beta \le 150$$

$$0.982\,\text{mA} \le I_C \le 1.0067\,\text{mA}$$

$$\therefore \frac{I_{C(\max)}}{I_{C(\min)}} = \frac{1.0067\,\text{mA}}{0.982\,\text{mA}} \cong 1.0254$$

Very good
Q-point
stability

Voltage Divider Bias Analysis

Transistor Saturation Level

$$I_{Csat} = I_{Cmax} = \frac{V_{CC}}{R_C + R_E}$$

Load Line Analysis

Cutoff:

$$V_{CE} = V_{CC}$$

$$I_C = 0\,\text{mA}$$

Saturation:

$$I_C = \frac{V_{CC}}{R_C + R_E}$$

$$V_{CE} = 0\,\text{V}$$

PNP Transistors

The analysis for *pnp* transistor biasing circuits is the same as that for *npn* transistor circuits. The only difference is that the currents are flowing in the opposite direction.

DC and AC Load Lines

Assume VCC $= 18\text{V}$, $\beta = 100$

$R_B = 576\,\text{k}\Omega$; $R_C = 3\text{k}\Omega$; $V_{BE} = 0.65\,\text{V}$

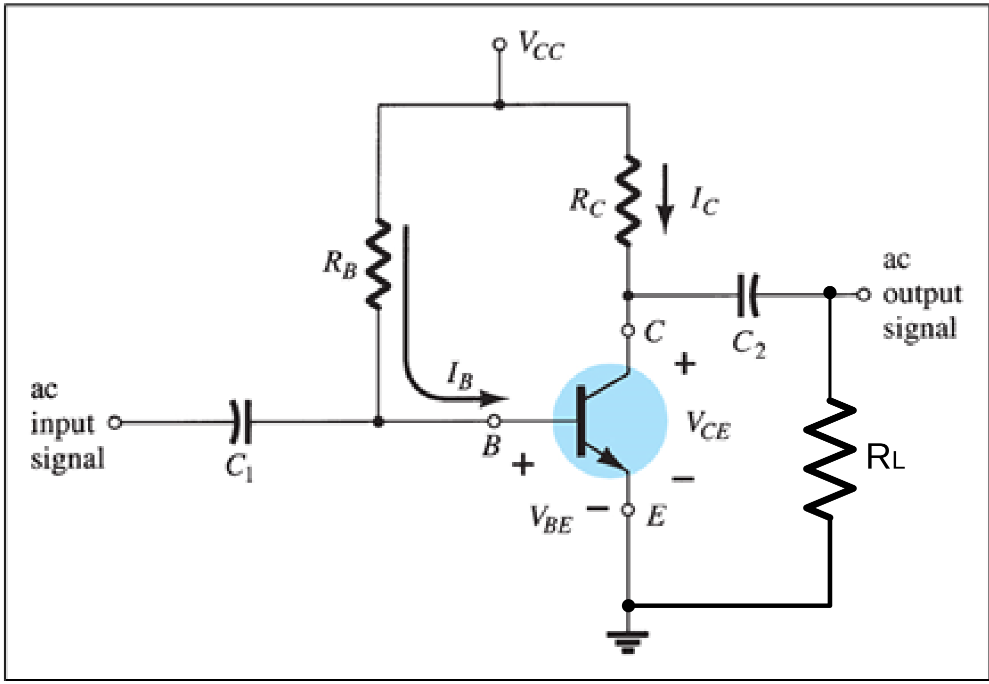
FIRST : DC ANALYSIS

$$V_{CC} = V_{CE} + I_C R_C$$

$$I_C = -\frac{1}{R_C} V_{CE} + \frac{V_{CC}}{R_C} \Leftarrow I_C = f(V_{CE})$$

This is a straight line equation

$$Y = mX + b$$



$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{18 - 0.65}{576\ \text{k}\Omega} = 30\,\mu\text{A}$$

$$I_C = \beta I_B = 3\,\text{mA}$$

$$V_{CE} = V_{CC} - I_C R_C = 18 - (3\text{mA})(3\text{k}\Omega)$$

$$= 9\,\text{V}$$

DC Load Line

I_{Csat}

$$I_{Csat} = \frac{V_{CC}}{R_C}$$

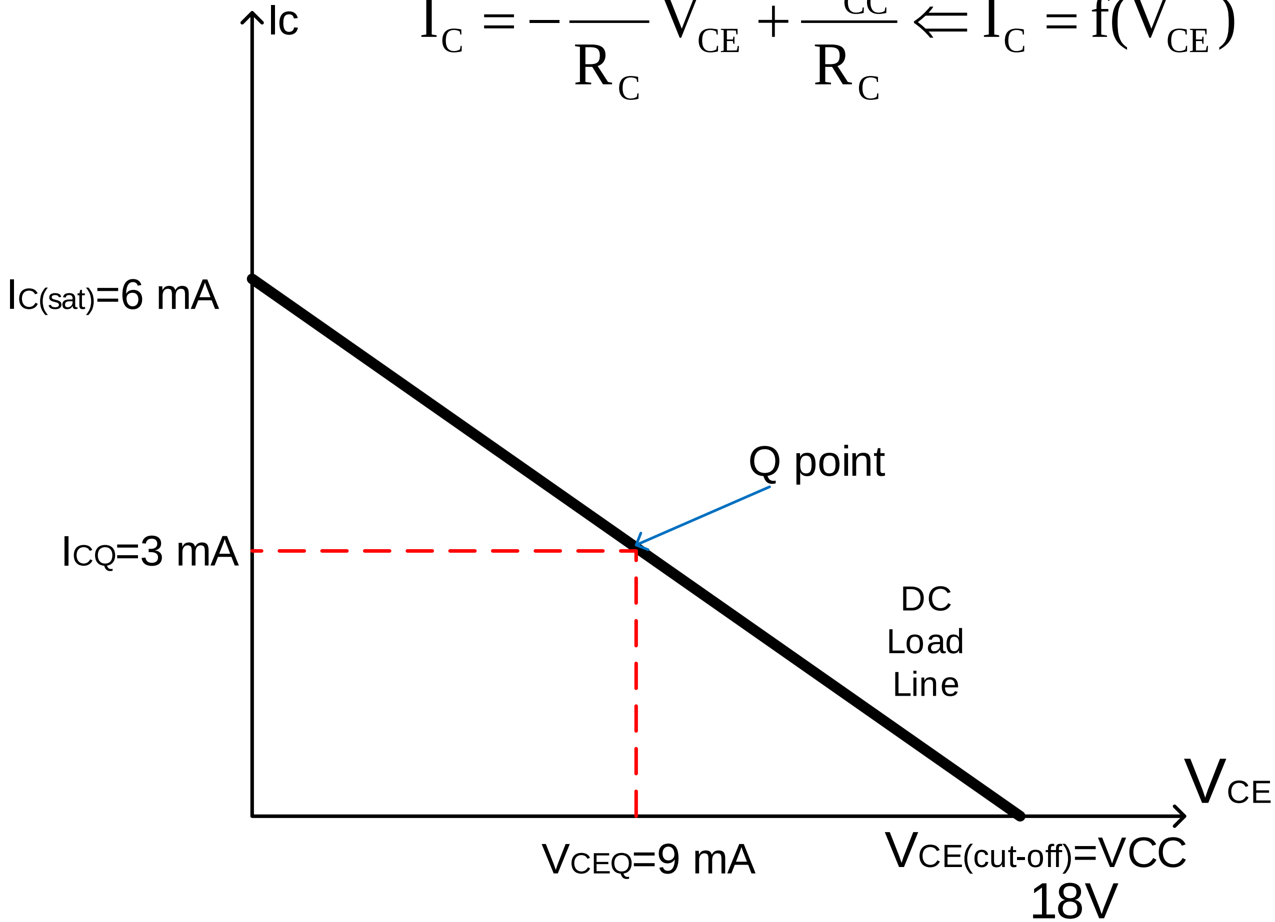
$$V_{CE} = V_{CE(sat)} \cong 0\ V$$

$V_{CEcutoff}$

$$V_{CE(cutoff)} = V_{CC}$$

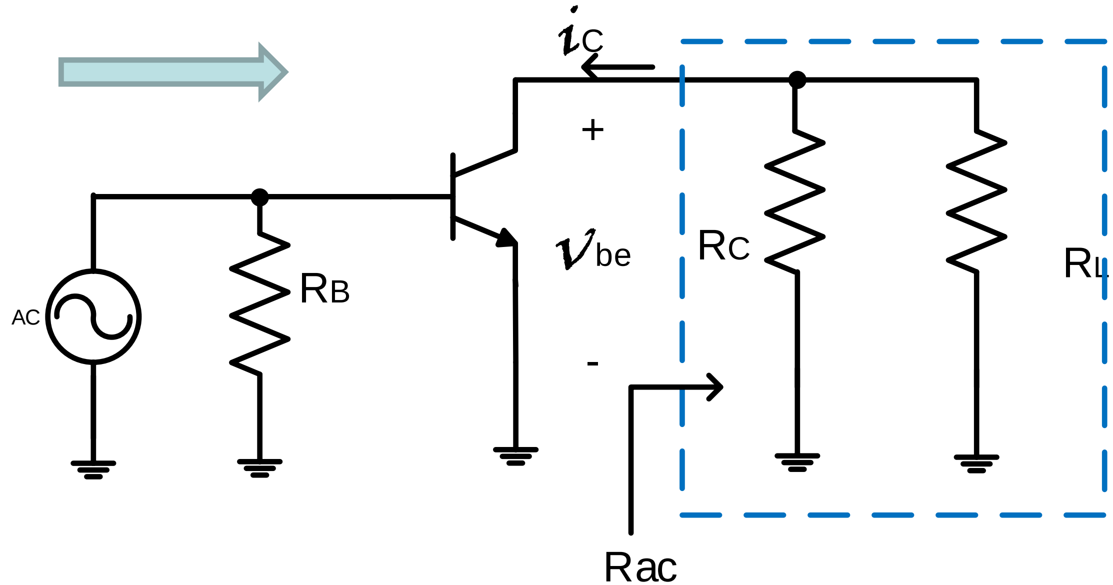
$$I_C = 0\ mA$$

$$I_C = -\frac{1}{R_C} V_{CE} + \frac{V_{CC}}{R_C} \Leftarrow I_C = f(V_{CE})$$



AC Load Line

AC Equivalent Circuit



Since we have dc and ac quantities,

let us define the notation

total DC ac

$$V_{BE}(t) = \mathrm{V_{BE}} + v_{be}$$

$$V_{CE}(t) = \mathrm{V_{CE}} + v_{ce}$$

$$I_C(t) = \mathrm{I_C} + i_c$$

$$I_B(t) = \mathrm{I_B} + i_b$$

$$v_{ce} = -R_{ac}.i_c$$

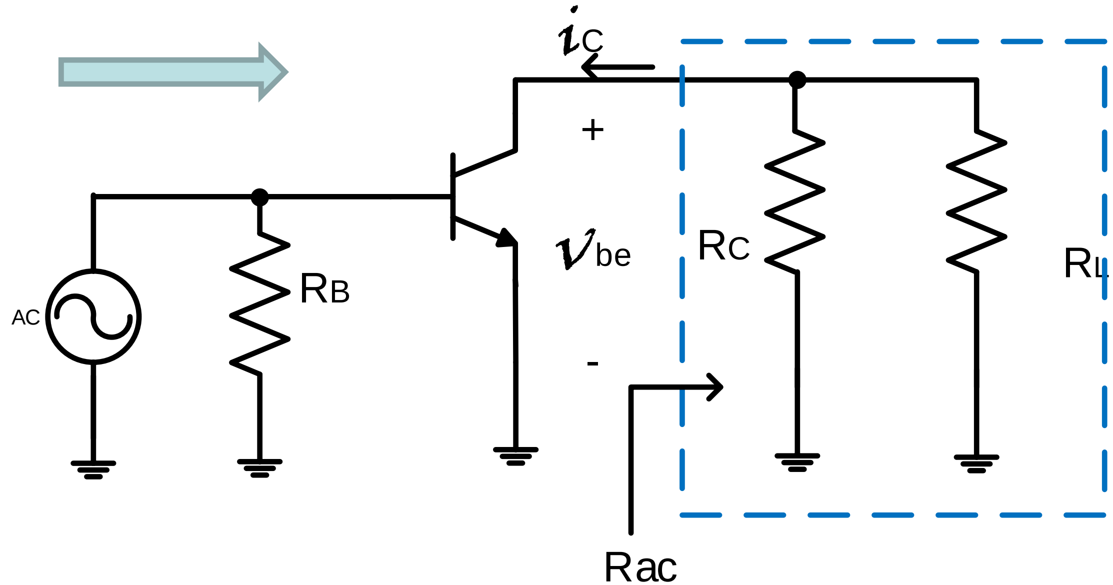
where $R_{ac} = R_c \,//\, R_L$

is the ac resistance seen from collector terminal

+ resistance seen from emitter terminal

AC Load Line

AC Equivalent Circuit



$$v_{ce} = V_{CE}(t) - \mathrm{V}_{\mathrm{CE}}$$

$$i_c = I_C(t) - \mathrm{I}_{\mathrm{C}}$$

$$v_{ce} = -R_{ac}.i_c$$

$$\left(V_{CE}(t) - \mathrm{V}_{\mathrm{CEQ}}\right) = -R_{ac}.\left(I_C(t) - \mathrm{I}_{\mathrm{CQ}}\right)$$

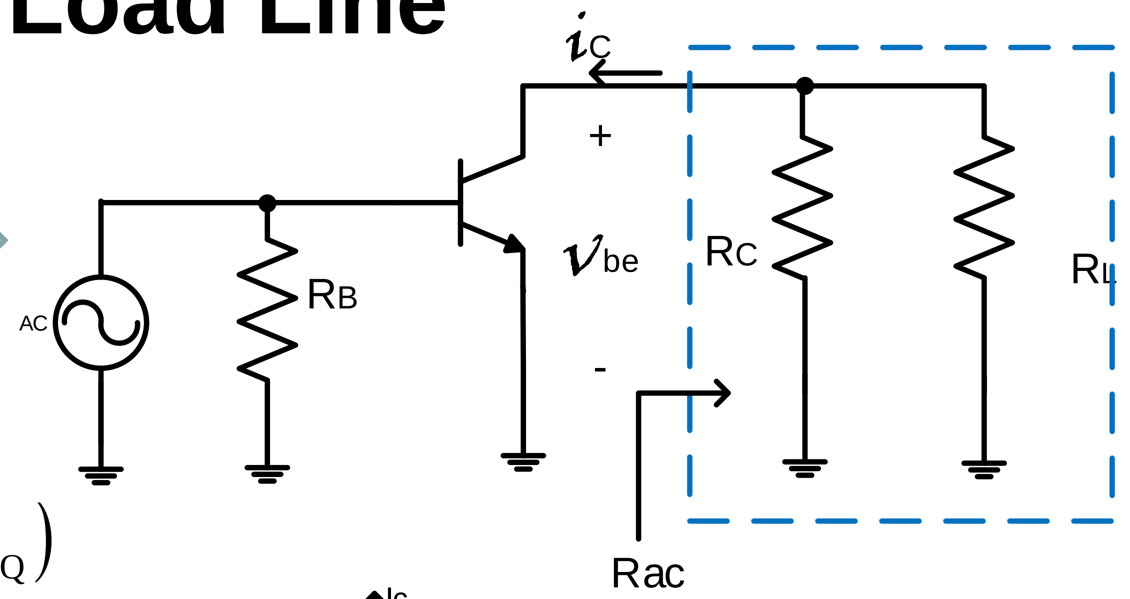
Ac load line equation

To Draw ac load line

we find $\left(V_{CE}(t)_{\max}\right)$ *and* $\left(I_C(t)_{\max}\right)$)

AC Load Line

AC Equivalent Circuit



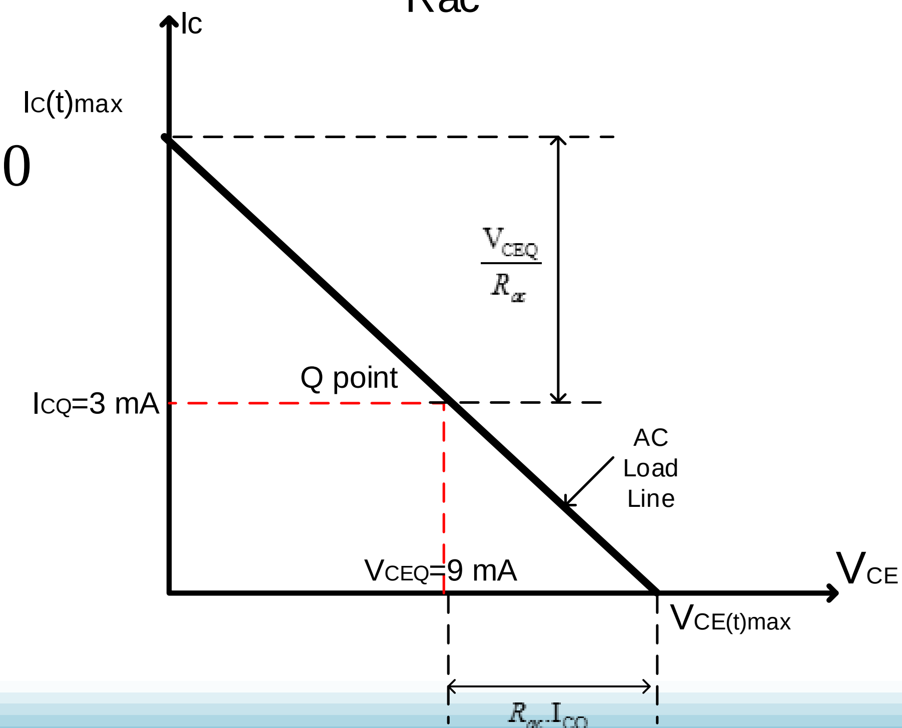
$$\left(V_{CE}(t) - \mathrm{V_{CEQ}}\right) = -R_{ac}.\left(I_C(t) - \mathrm{I_{CQ}}\right)$$

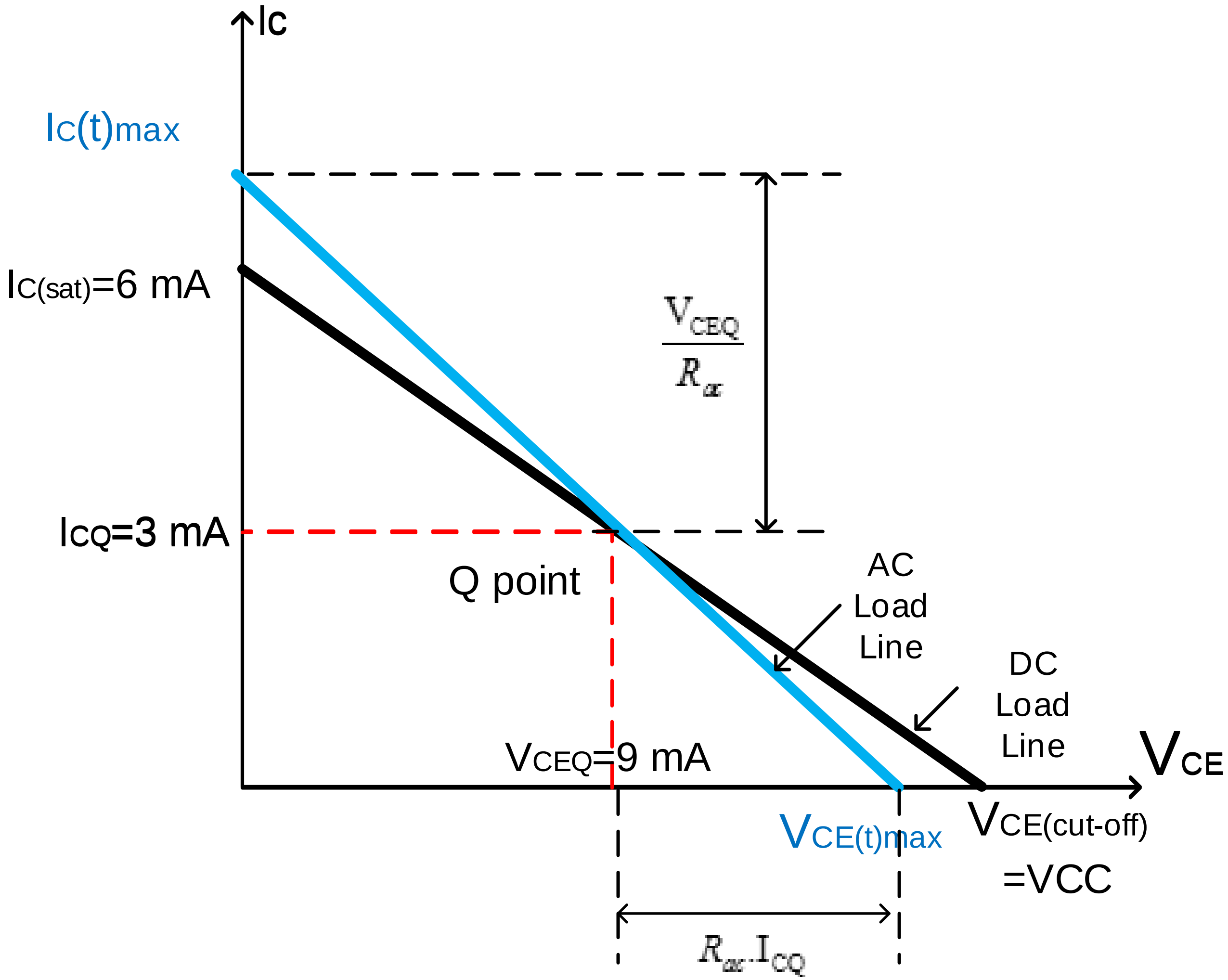
$$\left(V_{CE}(t)_{\max} - \mathrm{V_{CEQ}}\right) = R_{ac}.\mathrm{I_{CQ}}$$

$$V_{CE}(t)_{\max} = \mathrm{V_{CEQ}} + R_{ac}.\mathrm{I_{CQ}}\ , \text{ when } I_C(t) = 0$$

$$\left(V_{CE}(t) - \mathrm{V_{CEQ}}\right) = -R_{ac}.\left(I_C(t) - \mathrm{I_{CQ}}\right)$$

$$I_C(t)_{\max} = \frac{\mathrm{V_{CEQ}}}{R_{ac}} + \mathrm{I_{CQ}} \text{ when } V_{CE}(t) = 0$$





Ic
IC(t)max
IC(sat)=6 mA
VCEQ / Rac
ICQ=3 mA
Q point
AC Load Line
DC Load Line
VCEQ=9 mA
VCE
VCE(t)max
VCE(cut-off) =VCC
Rac.ICQ

Design

- In order to have the amplifier to amplify an input ac signal without distortion (by going into saturation or cut-off)
- We choose the Q-point in the middle of ac load line

$$I_{CQ} = \frac{1}{2} I_C(t)_{max}$$

$$V_{CEQ} = \frac{1}{2} V_{CE}(t)_{max}$$

$\Rightarrow$

$$2I_{CQ} = I_C(t)_{max}$$

$$2I_{CQ} = I_{CQ} + \frac{V_{CEQ}}{R_{ac}}$$

$$\therefore I_{CQ} = \frac{V_{CEQ}}{R_{ac}}$$

DC Analysis

$$V_{CC} = V_{CE} + I_C R_C$$
$$\text{define } R_{dc} = R_C$$
$$V_{CC} = V_{CE} + I_C R_{dc}$$

at the Q-point

$$V_{CC} = V_{CEQ} + I_{CQ} R_{dc}$$

For maximum Symmetrical swing

$$I_{CQ} = \frac{V_{CEQ}}{R_{ac}} \Rightarrow V_{CEQ} = I_{CQ} R_{ac}$$

$$V_{CC} = I_{CQ}.R_{ac} + I_{CQ}.R_{dc}$$

$$\therefore I_{CQ} = \frac{V_{CC}}{R_{ac} + R_{dc}}$$

To design for maximum Symmetrical Swing

DC Analysis

Also

$$V_{CEQ} = V_{CC} - I_{CQ}R_{dc}$$

$$= V_{CC} - R_{dc}\frac{V_{CC}}{R_{ac} + R_{dc}}$$

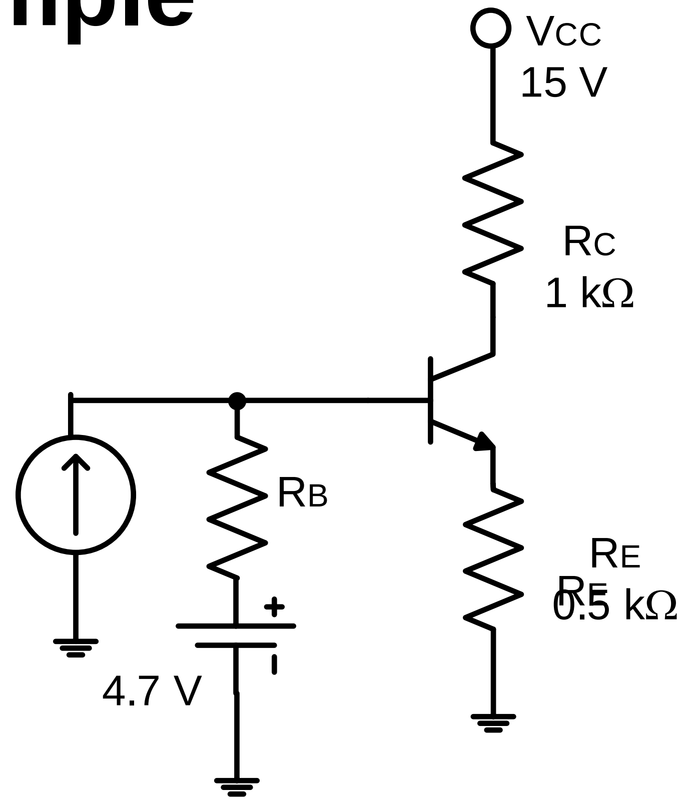
$$= V_{CC}\left(1 - \frac{R_{dc}}{R_{ac} + R_{dc}}\right)$$

$$= V_{CC}\left(\frac{R_{ac} + R_{dc} - R_{dc}}{R_{ac} + R_{dc}}\right)$$

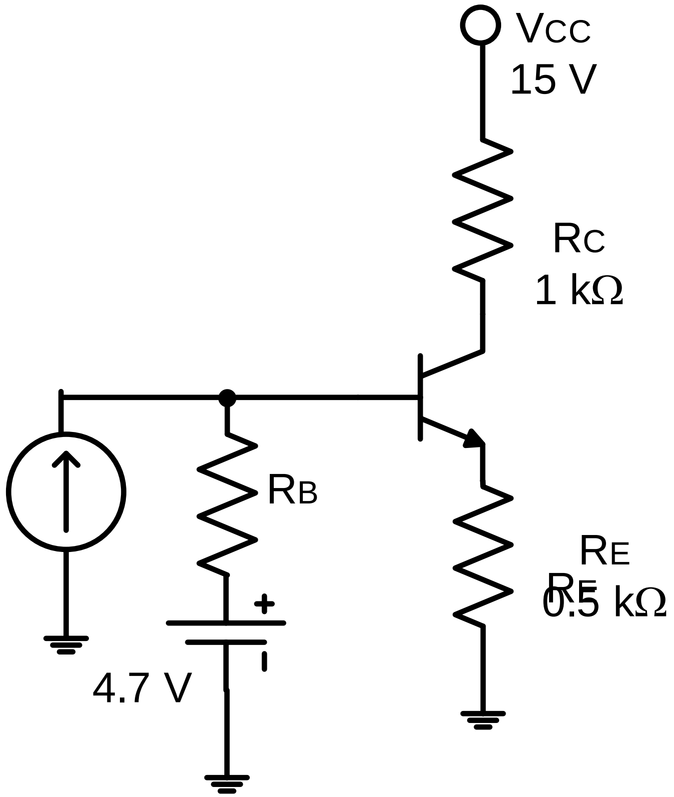
$$= V_{CC}\left(\frac{R_{ac}}{R_{ac} + R_{dc}}\right) = \left(\frac{V_{CC}}{1 + \frac{R_{dc}}{R_{ac}}}\right)$$ *****For maximum Symmetrical swing

Design Example

Design for maximum symmetrical swing of the collector current? Find the Q-point?
Find the required Value of R_B?
Draw AC and DC load lines
What is the power dissipation of the transistor at the Q-point?



Solution



$$R_{ac} = R_C = 1\ k\Omega$$

$$R_{dc} = R_C + R_E = 1.5\ k\Omega$$

For Maximum Symmetrical Swing of Ic

$$I_{CQ} = \frac{V_{CC}}{R_{ac} + R_{dc}} = \frac{15}{1\ k\Omega + 1.5\ k\Omega} = 6\ mA$$

$$V_{CEQ} = \frac{V_{CC}}{1 + \frac{R_{dc}}{R_{ac}}} = \frac{15}{1 + \frac{1.5\ k\Omega}{1\ k\Omega}} = 6\ V$$

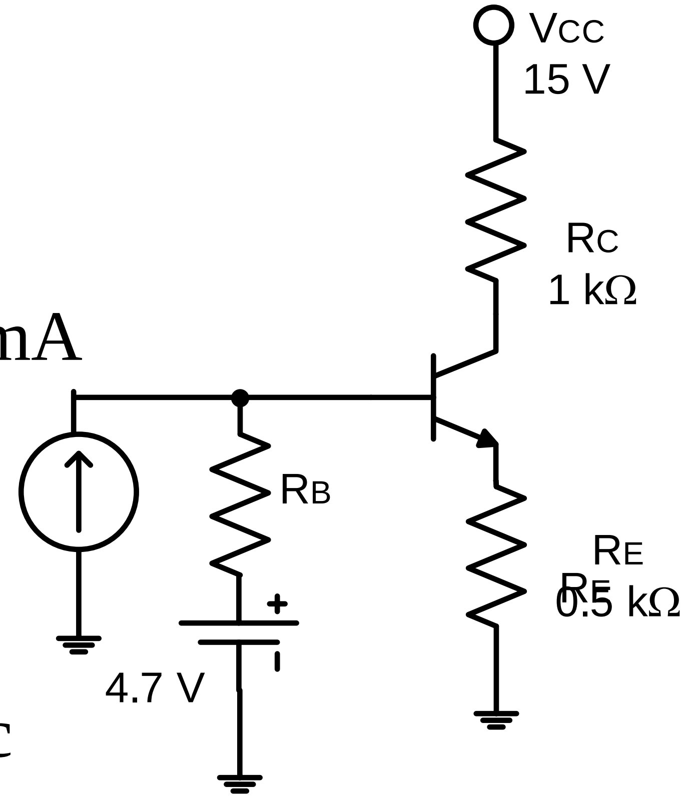
Maximum Swing (peak) of Ic

$$I_{CM} = I_{CQ} = 6\ mA$$

Maximum Symmetrical Swing (peak - peak) of Ic

$$I_{Cp\text{-}p} = 2I_{CQ} = 12\ mA$$

Solution



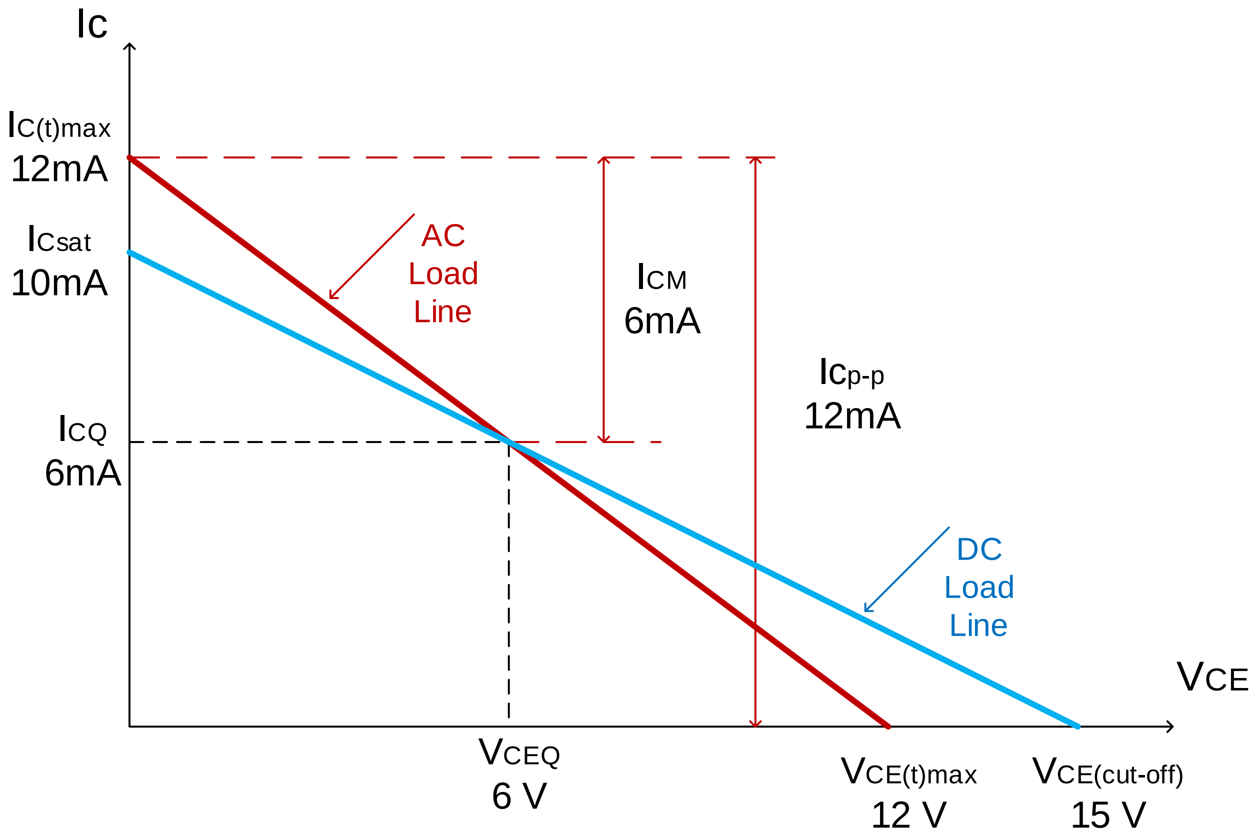
For Maximum Symmetrical Swing of Ic

$$I_C(t)_{Max} = I_{CQ} + \frac{V_{CEQ}}{R_{ac}} = 6\,mA + \frac{6}{1\ k\Omega} = 12\,mA$$

For Maximum Symmetrical Swing of Ic

$$V_{CE}(t)_{Max} = I_{CQ}R_{ac} + V_{CEQ} = 6\,mA.1\ k\Omega + 6 = 12\ V$$

Example -Continued



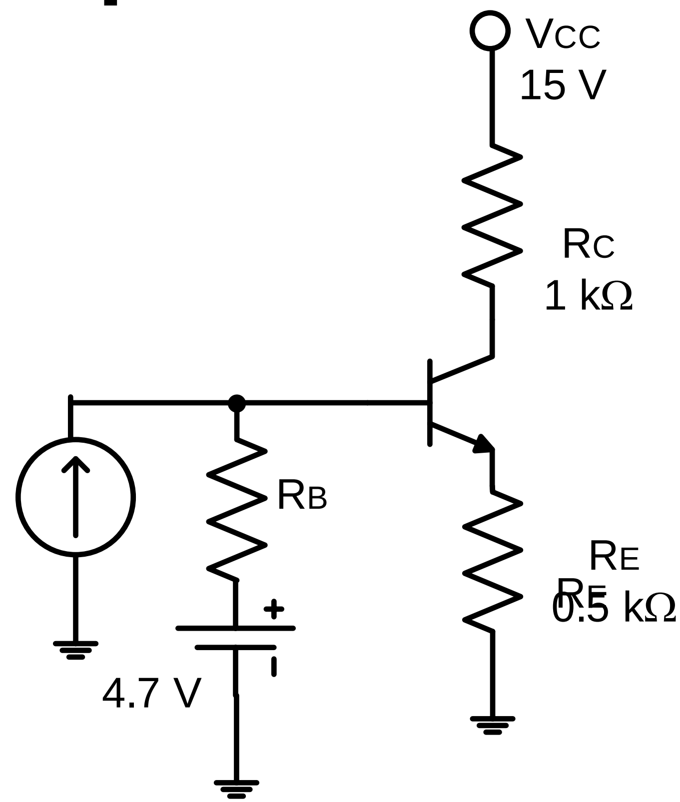
$$I_B = \frac{4.7 - 0.7}{R_E(100+1) + R_B} = \frac{I_{CQ}}{100} = 60\,\mu A$$

$$\therefore R_B = 33\,k\Omega$$

$$P_Q = V_{CEQ}.I_{CQ} = 6V.\,6mA = 36\,mW$$

Analysis Example

R_B=50 kΩ
Find the maximum collector current swing and the Q-point?
Draw AC and DC load lines
What is the power dissipation of the transistor at the Q-point?



Solution

$$R_{ac} = R_C = 1\ \text{k}\Omega$$

$$R_{dc} = R_C + R_E = 1.5\ \text{k}\Omega$$

Value of Ic

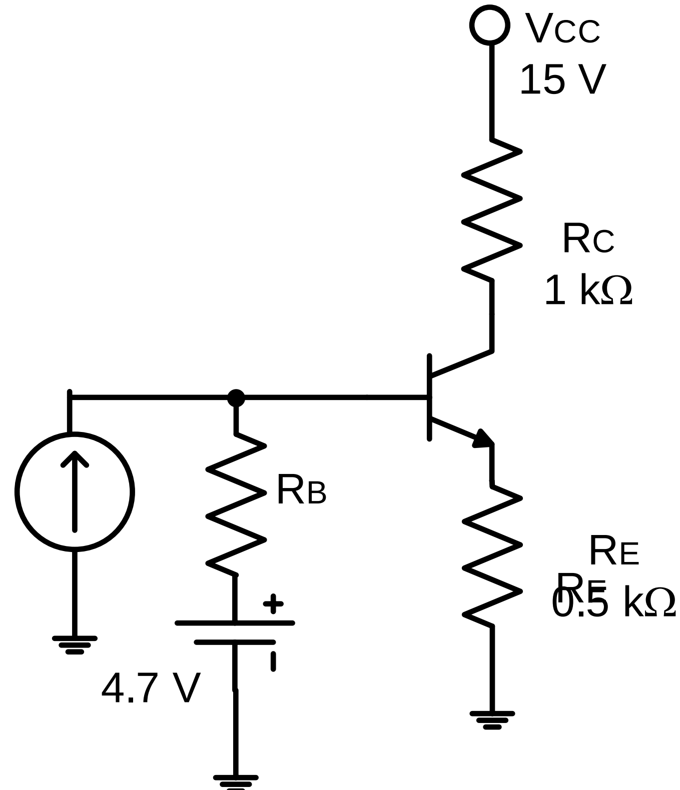
$$I_B = \frac{4.7 - 0.7}{R_E(100+1) + R_B}$$

$$= \frac{4.7 - 0.7}{500(100+1) + 50\text{k}\Omega}$$

$$= 40\ \mu\text{A}$$

$$I_{CQ} = \beta I_{BQ} = 4\ \text{mA}$$

$$V_{CEQ} = V_{CC} - I_{CQ}\left(R_C + R_E\right) = 9\ \text{V}$$



Maximum Swing (peak) of Ic

$$I_{CM} \neq I_{CQ}$$

$$I_{CM} = 4\ \text{mA}$$

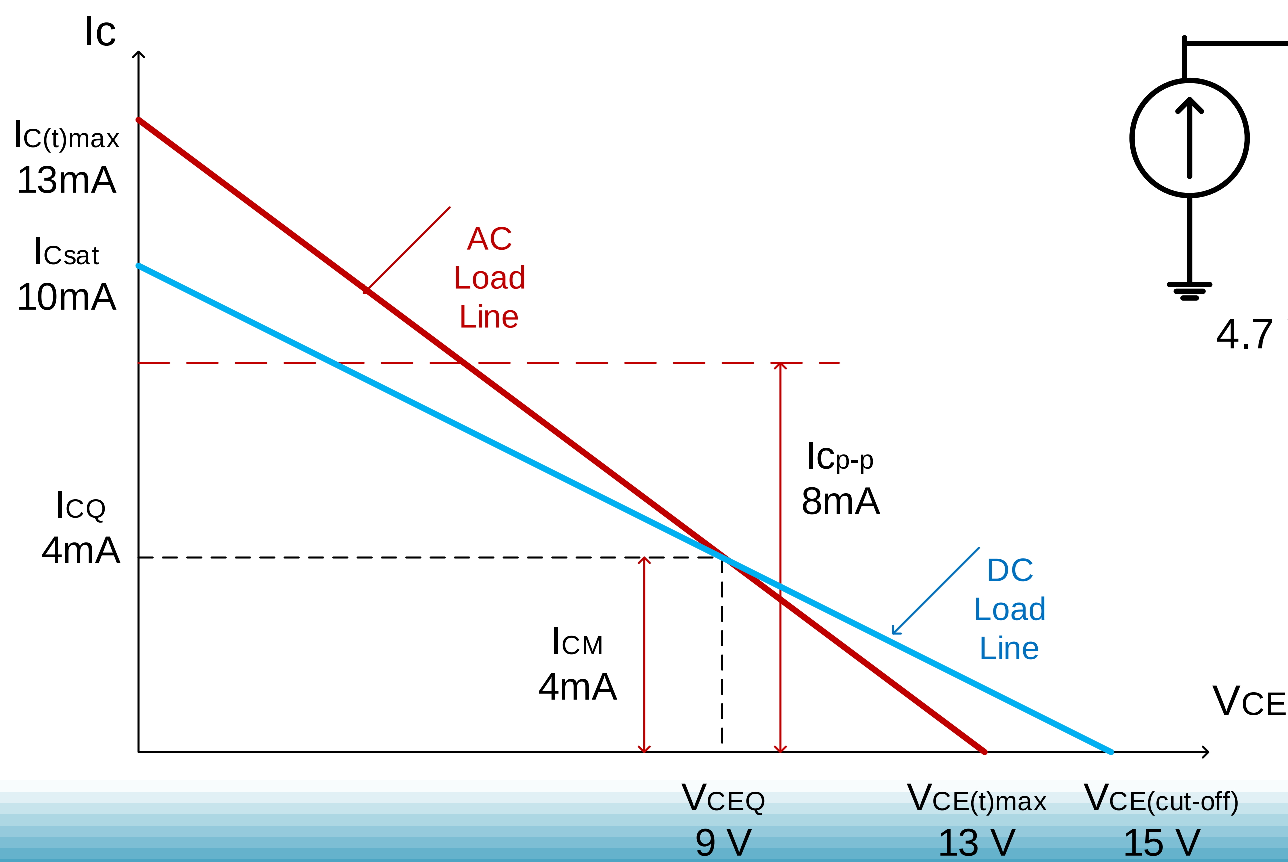
Maximum Symmetrical Swing (peak-peak) of Ic

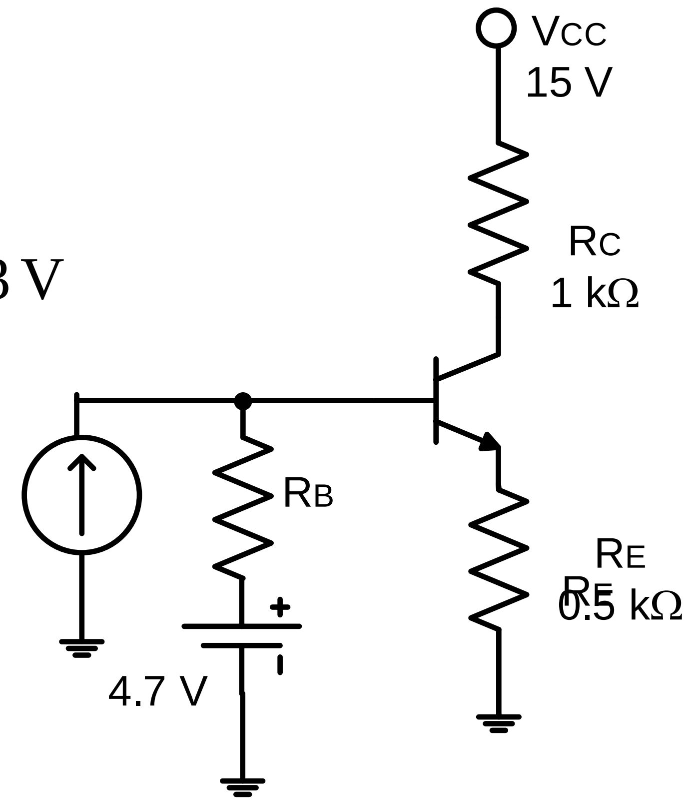
$$I_{Cp\text{-}p} = 2I_{CM} = 8\ \text{mA}$$

Solution

$$I_C(t)_{Max} = I_{CQ} + \frac{V_{CEQ}}{R_{ac}} = 4\,\text{mA} + \frac{9}{1\ \text{k}\Omega} = 13\,\text{mA}$$

$$V_{CE}(t)_{Max} = I_{CQ}R_{ac} + V_{CEQ} = 4\,\text{mA}.1\ \text{k}\Omega + 9 = 13\,\text{V}$$





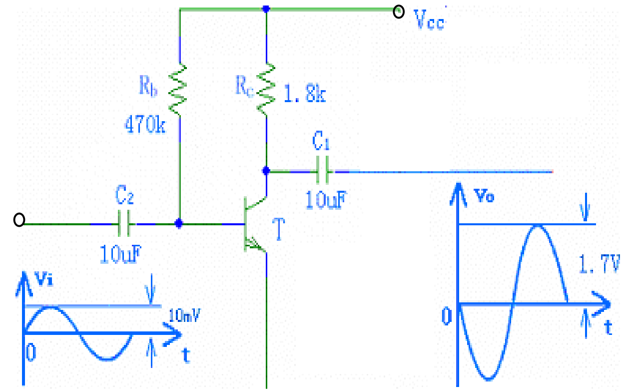
Maximum Swing was reduced because the Q-point was not placed properly

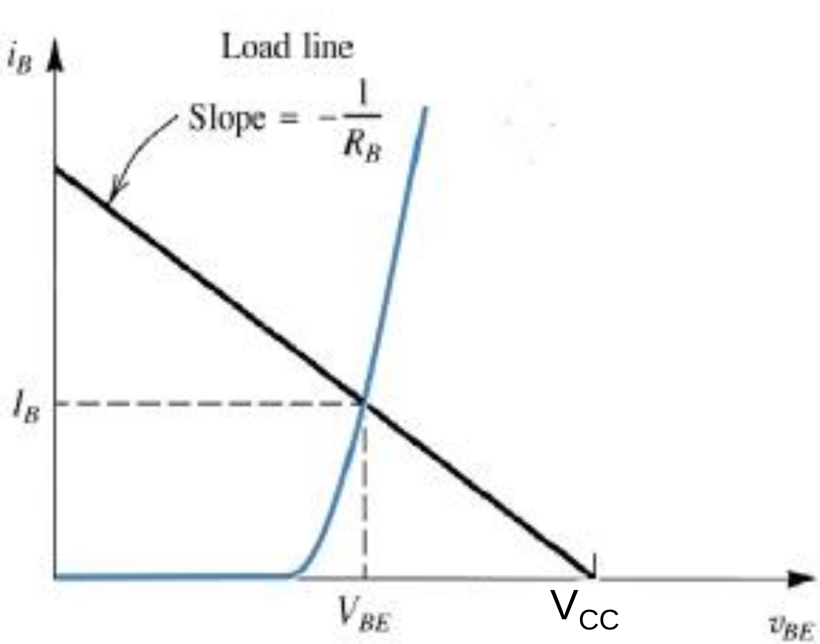
Example -Continued

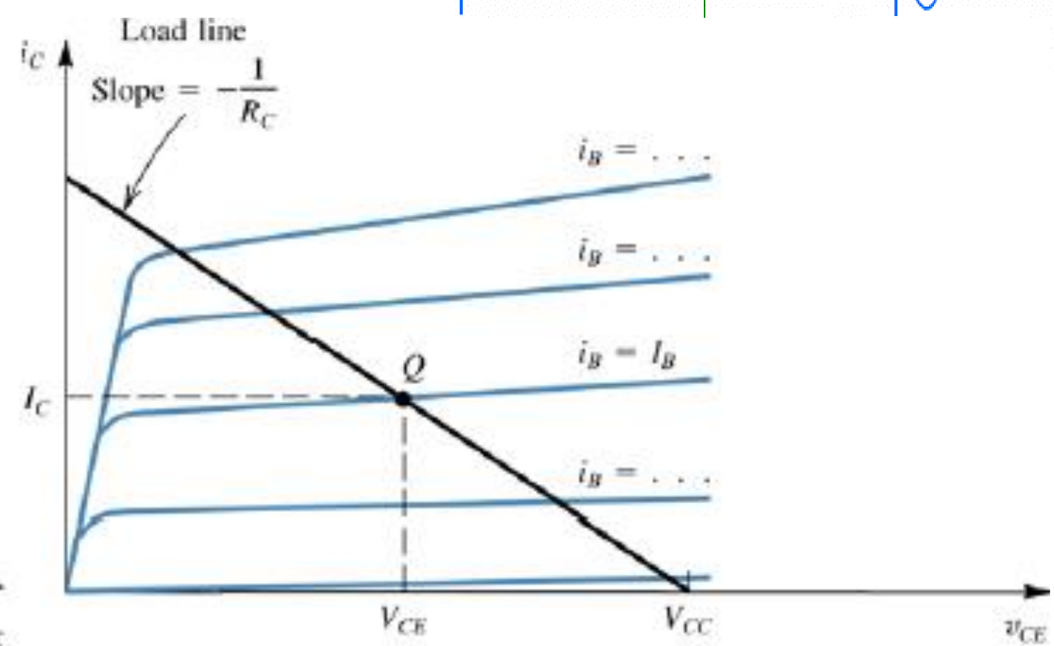
Basic BJT Amplifiers Circuits

Graphical Analysis

- Can be useful to understand the operation of BJT circuits.
- First, establish DC conditions by finding I_B (or V_{BE})
- Second, figure out the DC operating point for I_C





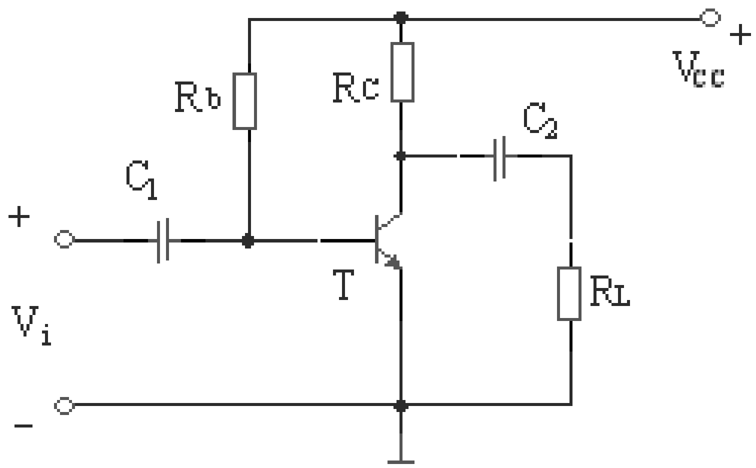


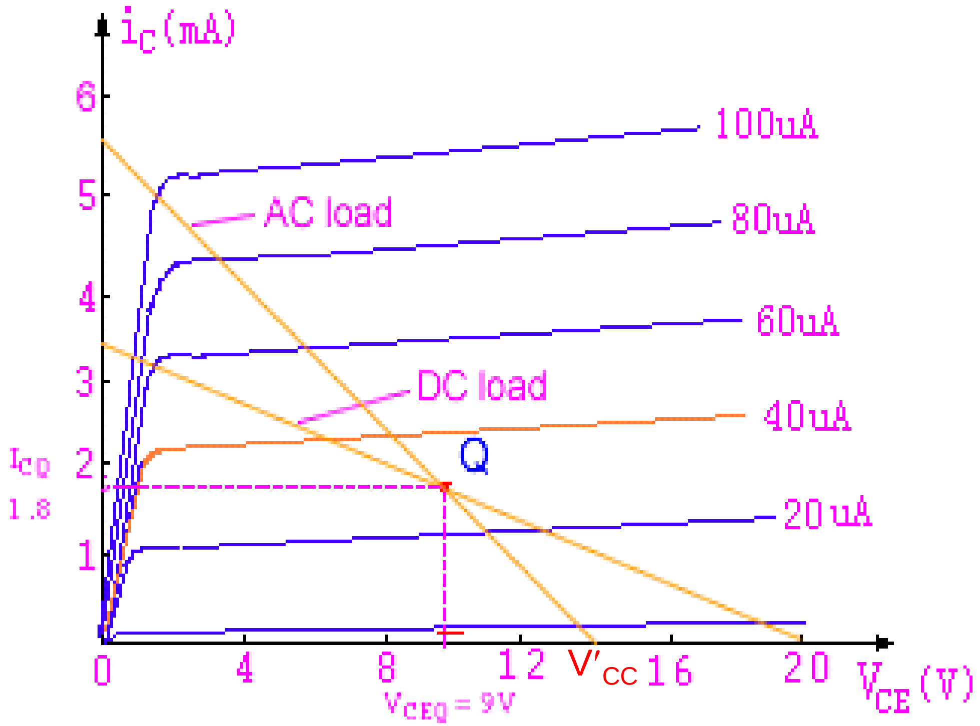
Can get a feel for whether the BJT will stay in active region of operation

– What happens if R_C is larger or smaller?

Basic BJT Amplifiers Circuits

Graphical Analysis

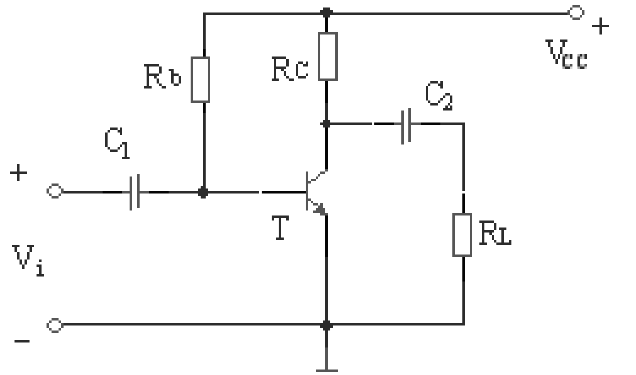




$$v_{ce} = -i_c (R_C // R_L) = -i_c R_L^{'}$$

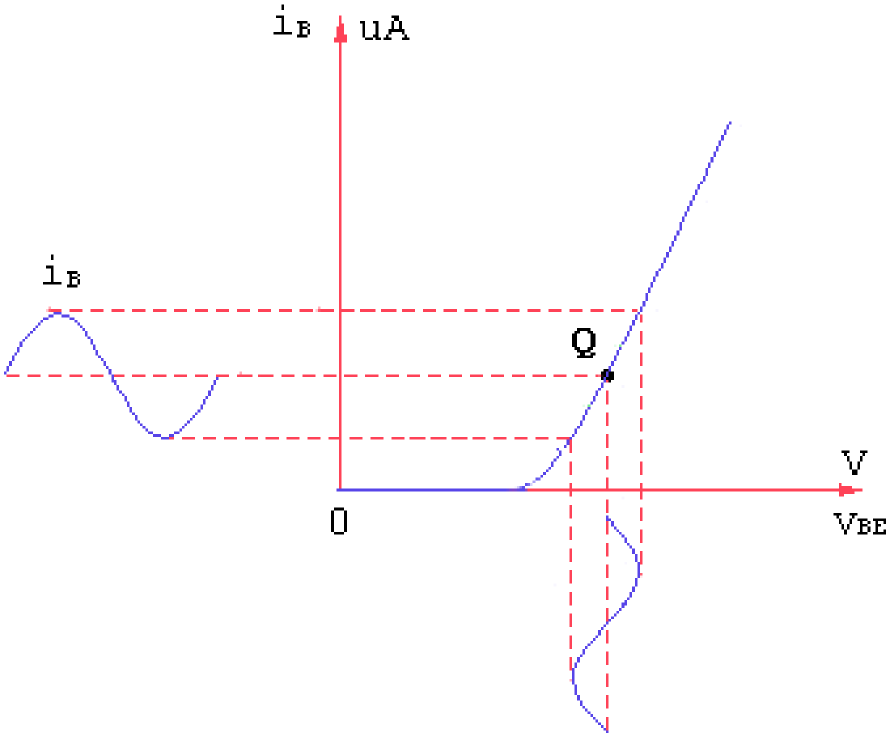
$$V_{CC}' = V_{CEQ} + I_{CQ} R_L'$$

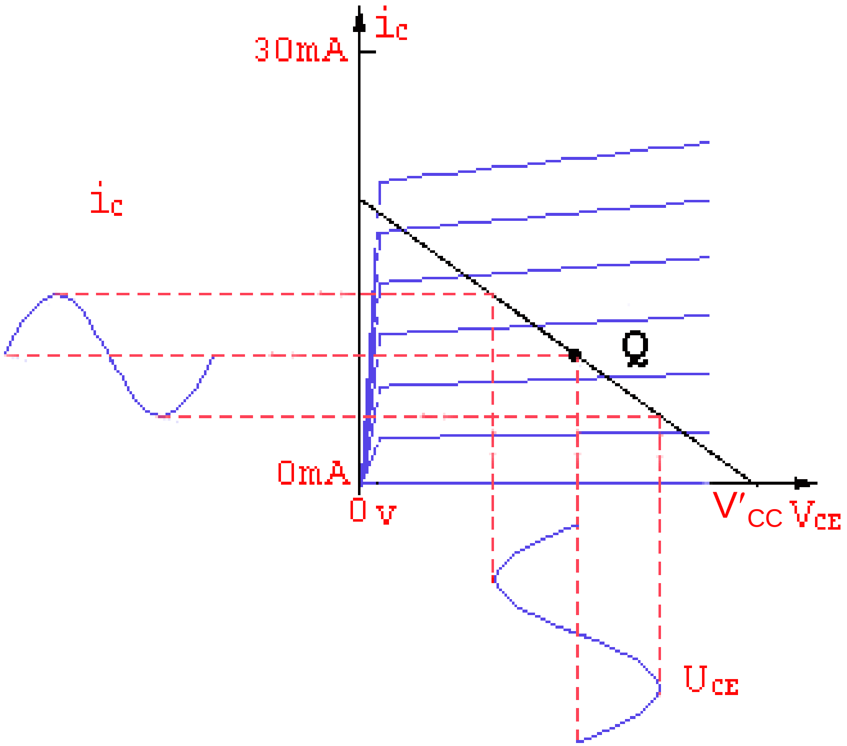
Basic BJT Amplifiers Circuits



Graphical Analysis

Q-point is centered on the ac load line:

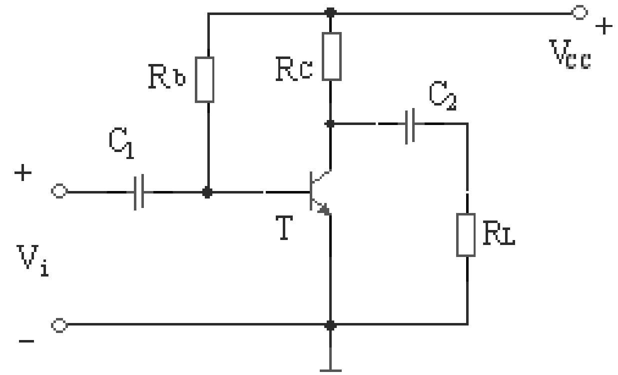


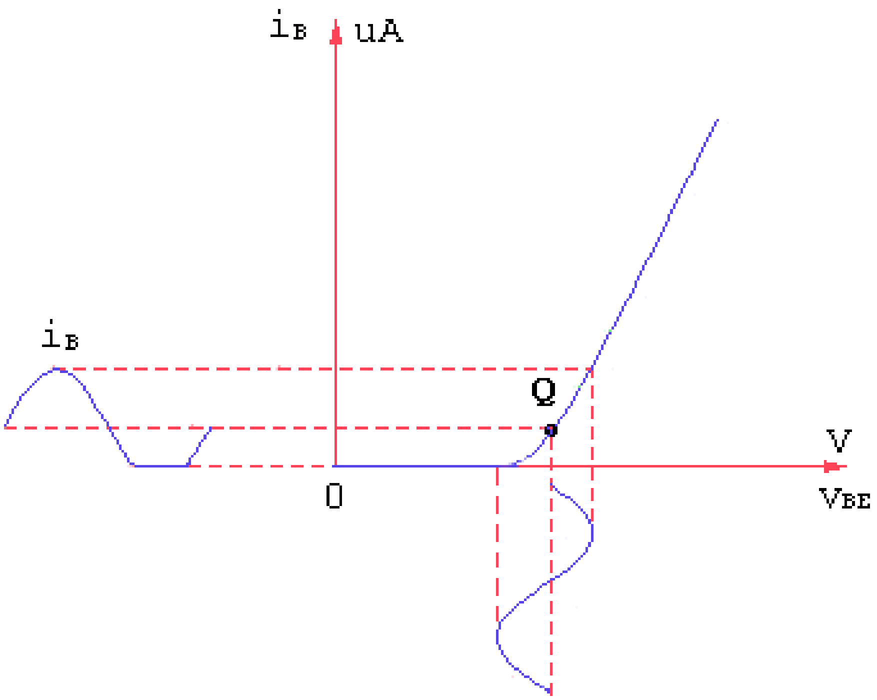


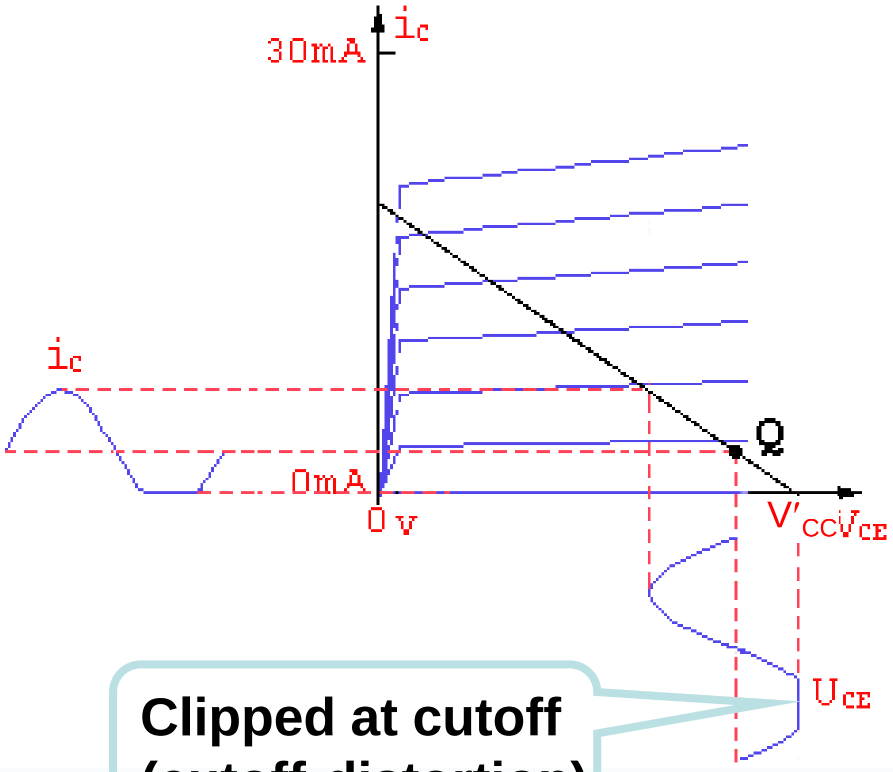
Basic BJT Amplifiers Circuits

Graphical Analysis

Q-point closer to cutoff:







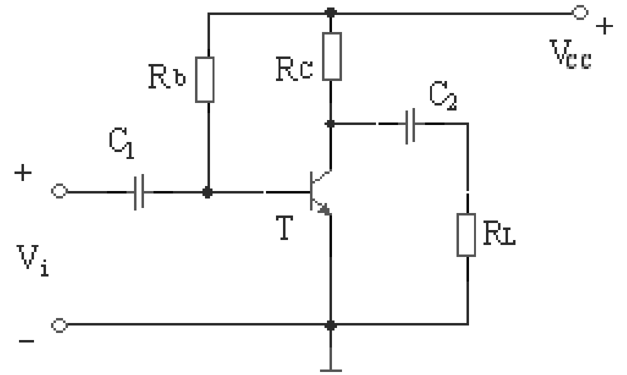
Clipped at cutoff (cutoff distortion)

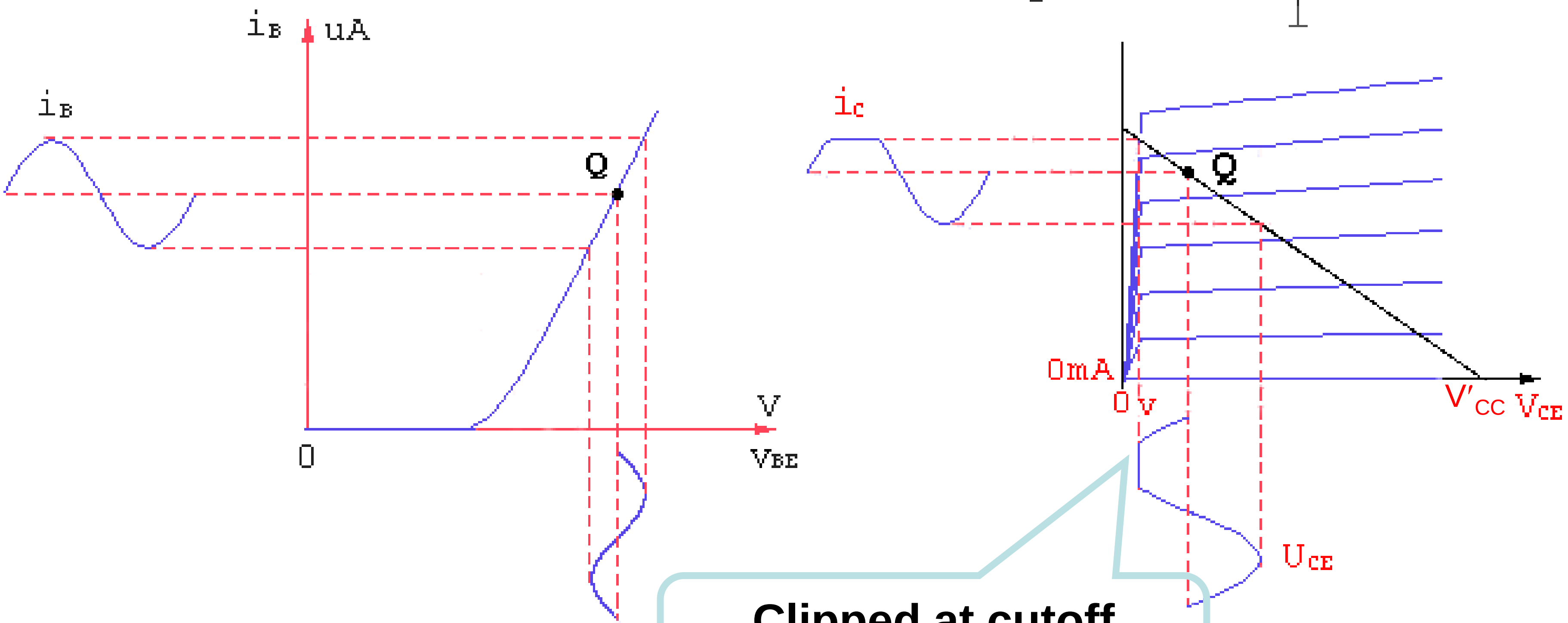
Basic BJT Amplifiers Circuits

6.2 Single-Stage BJT Amplifiers

Graphical Analysis

Q-point closer to saturation:

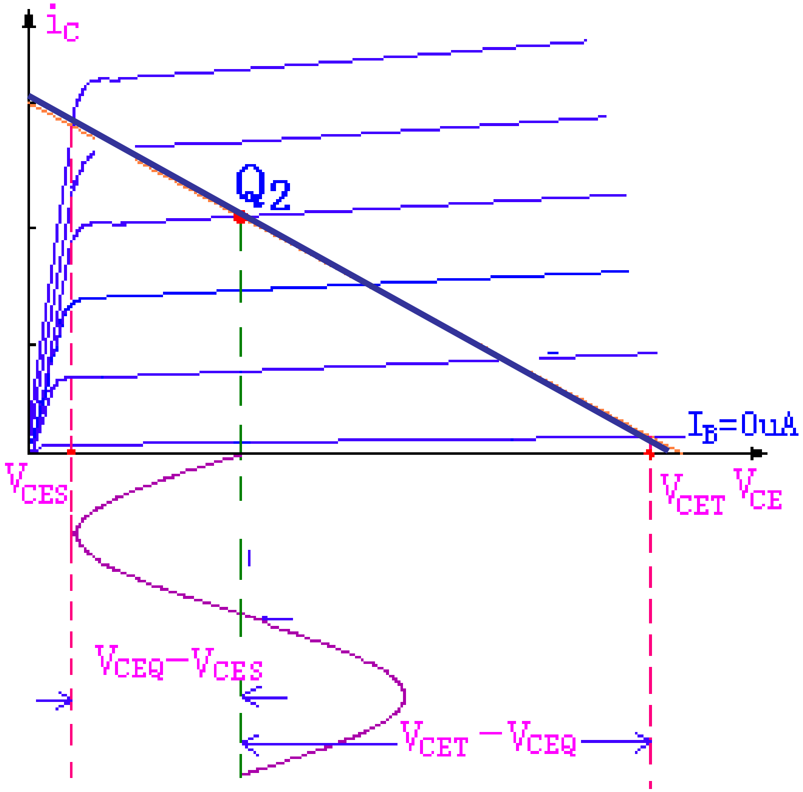


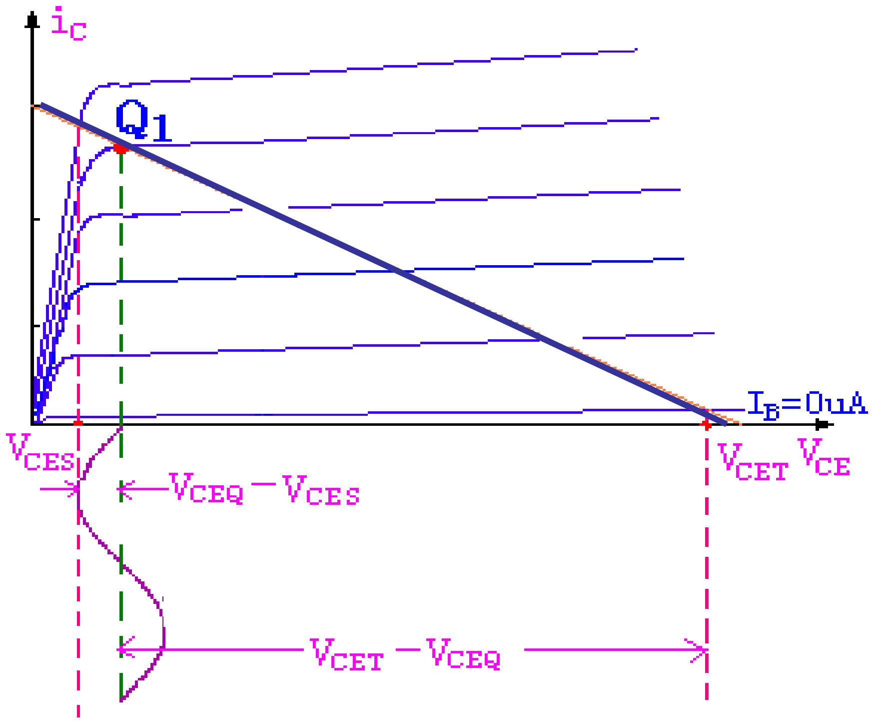


Clipped at cutoff
(saturation distortion)

Basic BJT Amplifiers Circuits

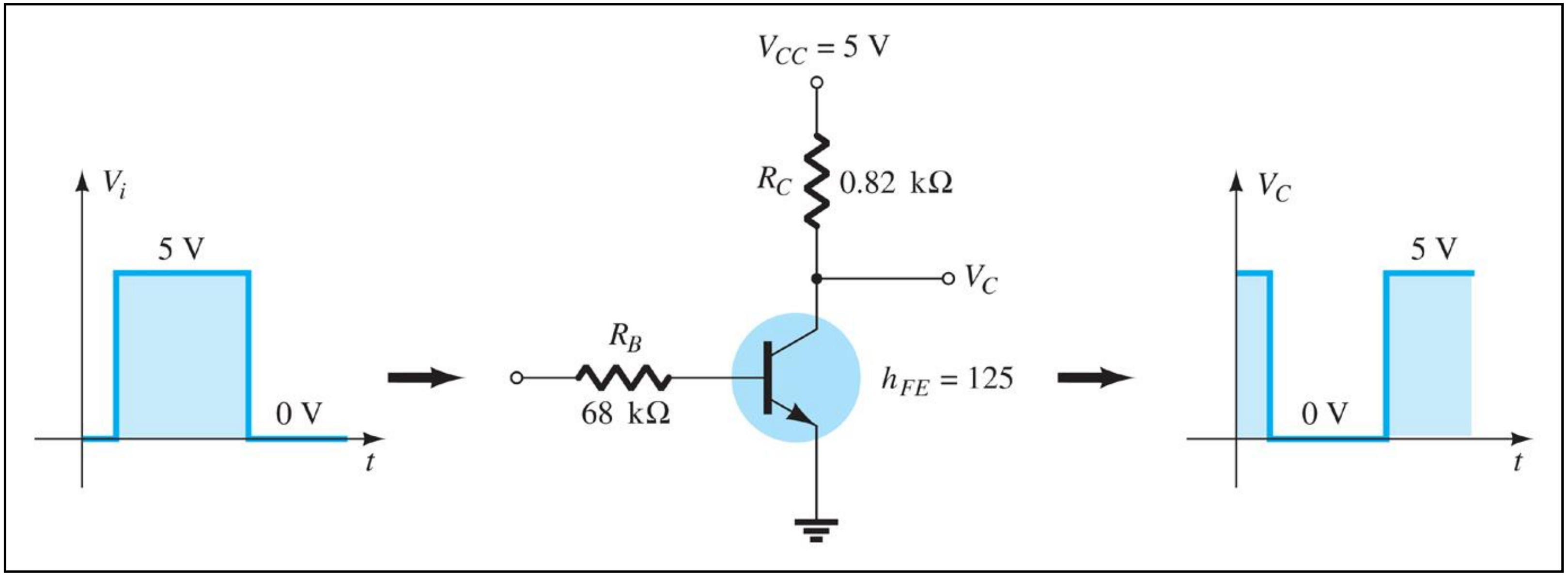
Graphical Analysis





Transistor Switching Networks

Transistors with only the DC source applied can be used as electronic switches.



For Vi = 5V

$$I_B = \frac{5 - 0.7}{68k\Omega} = 63.24\ \mu A$$

$$I_C = (125)(63.24\ \mu A) = 7.9\ mA$$

$$V_{CE} = V_{CC} - I_C R_C$$

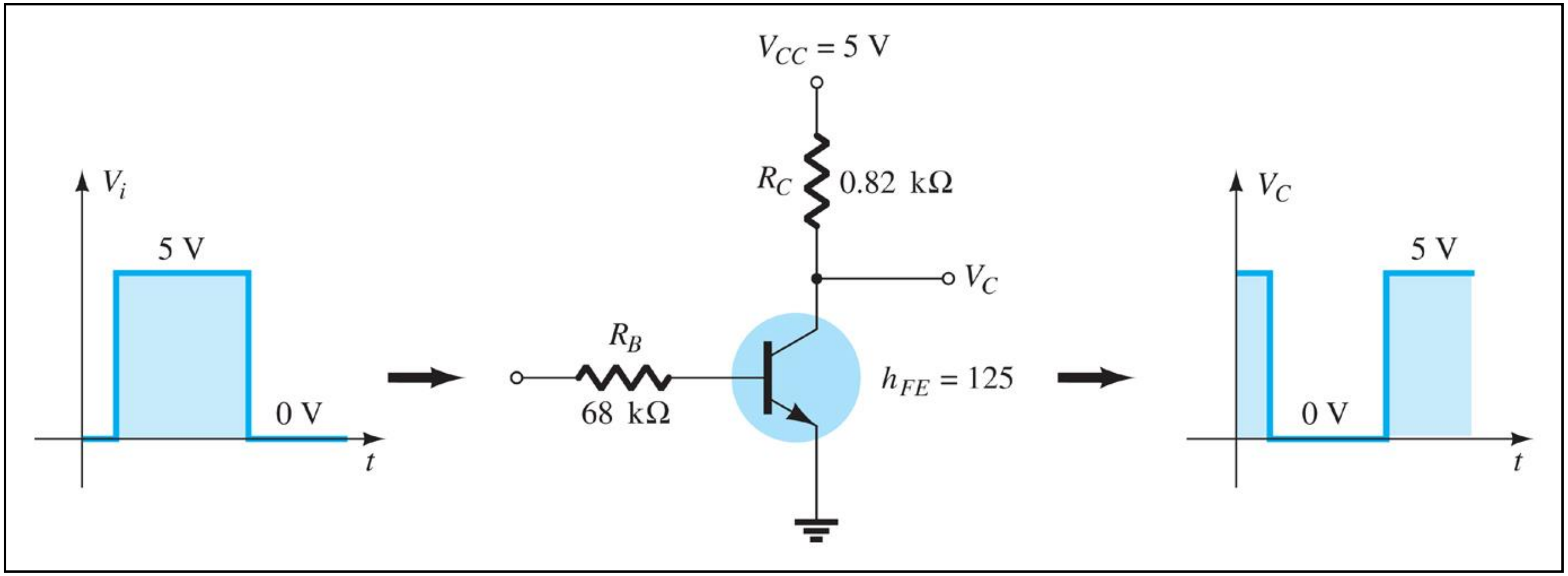
$$= 5 - (7.9\ mA)(0.82k\Omega)$$

$$= -1.482V < V_{CE(sat)}$$

$$\therefore \text{BJT is in Sat. Mode \& } Vc = V_{CE(sat)}$$

Transistor Switching Networks

Transistors with only the DC source applied can be used as electronic switches.

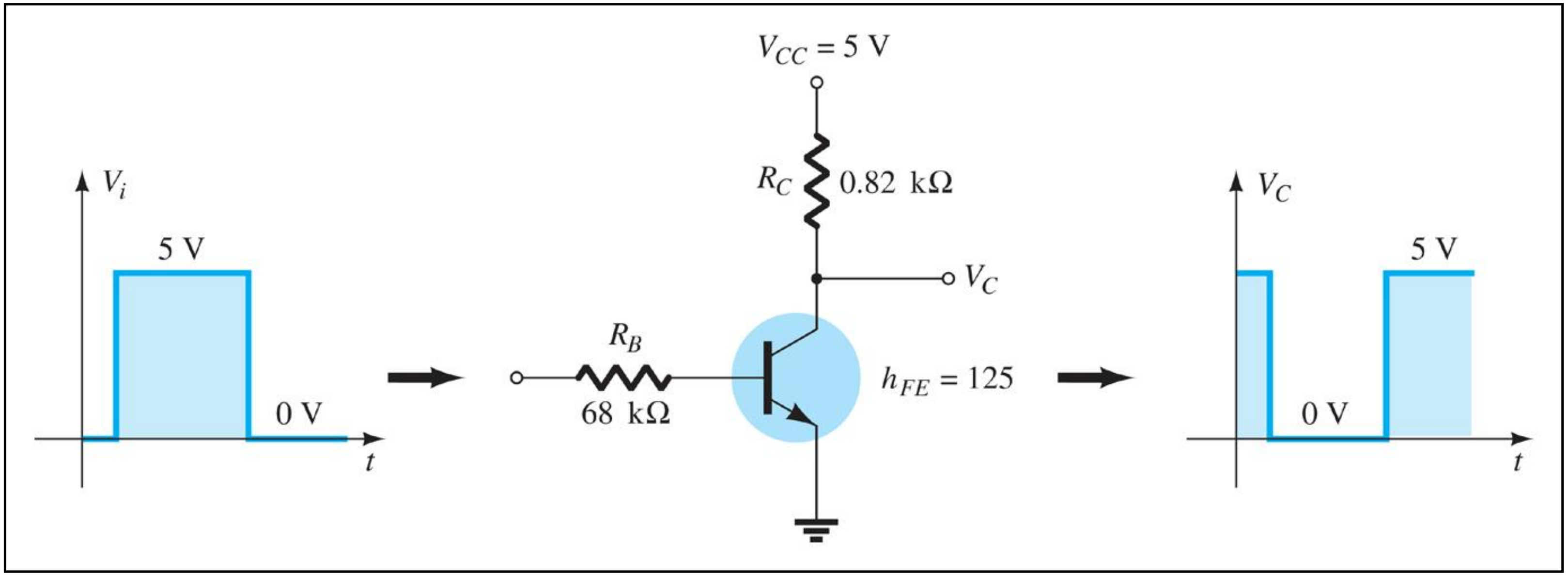


$$I_{C(sat)} = \frac{5}{0.82\,k\Omega} = 6.1\,mA$$

$$Vo = V_{CE(sat)} \cong 0.2\,V$$

Transistor Switching Networks

Transistors with only the DC source applied can be used as electronic switches.



$$\text{For Vi} = 0\text{V}$$

$$I_B = 0$$

$$I_C = 0$$

$$V_{CE} = V_{CC}$$

$$\therefore \text{BJT is in Cut-off Mode \& Vc} = V_{CE(cut0ff)} = V_{CC} = 5V$$